

Compal Confidential

Model Name : VITU5

File Name : LA-8971P

# Compal Confidential

## VITU5 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH(HM77)

Nvidia chip:N13M-GS(23x23)

2012-02-16

REV : 0 . 1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Voltage Rails				
power plane	+B	+5VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG
State		+3VALW		+1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address		EC SM Bus2 address	
Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor F75303M	1001_101xb

PCH SM Bus address	
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

AMD-GPU SM Bus address	
Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table								
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB 3.0	USB 2.0		Port	3 External USB Port
xHCI1	EHCI1	UHCI0	0	USB 3.0 Port (Left Side)
xHCI2			1	
xHCI3		UHCI1	2	USB/B (Right Side USB-BD)
xHCI4			3	USB/B (Right Side USB-BD)
		UHCI2	4	X (USB PORT disabled on HM70 )
			5	X (USB PORT disabled on HM70 )
	EHCI2	UHCI3	6	X (USB PORT disabled on HM70 )
			7	X (USB PORT disabled on HM70 )
		UHCI4	8	Camera
			9	Blue Tooth
		UHCI5	10	Mini Card(WLAN)
			11	USB Port (Right Side CR-BD)
		UHCI6	12	X (USB PORT disabled on HM70 )
			13	X (USB PORT disabled on HM70 )

HM70 Disable xHCI3,xHCI4

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel						
Vcc	3.3V +/- 5%					
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

BTO Item	BOM Structure
INTEL UMA only	UMA@
GPU:Seymour XTX	XTX@
HDMI	HDMI@
HDD1 (HM77 SATA 3.0)	HDD1@
HDD2 (HM70 SATA 2.0)	HDD2@
Interna-Intel-USB3.0	IU3@
Interna-Intel-USB2.0	IU2@
Blue Tooth	BT@
10/100 LAN	8105E@
GIGA LAN	8111F@
Connector	ME@
45 LEVEL	45@
Unpop	@

	HM77	HM70	
SATA P0	GEN3/2/1	GEN3/2/1	SSD
SATA P1	GEN3/2/1	Disable	HDD (HM77)
SATA P2	GEN2/1	GEN2/1	HDD (HM70)
SATA P3	GEN2/1	Disable	
SATA P4	GEN2/1	GEN2/1	
SATA P5	GEN2/1	GEN2/1	

HM70 Disable P1,P3

	HM77	HM70	
PCie P1	Enable	Enable	LAN
PCie P2	Enable	Enable	WLAN
PCie P3	Enable	Enable	
PCie P4	Enable	Enable	
PCie P5	Enable	Disable	
PCie P6	Enable	Disable	
PCie P7	Enable	Disable	
PCie P8	Enable	Disable	

HM70 Disable P5,P6,P7,P8

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Hot plug detect for IFP link C

## VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	

## Performance Mode P0 TDP at Tj = 102 C\* (GDDR3)

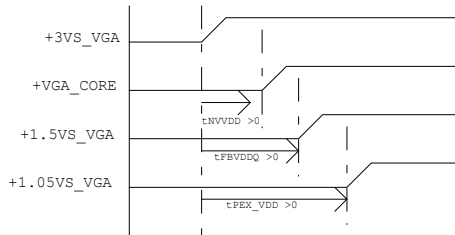
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

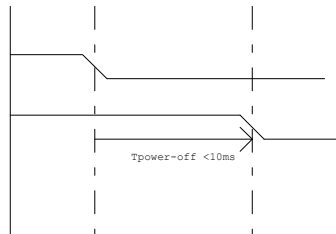
	Device ID
N13P-GL (28nm)	???
N13M-GE (28nm)	???

GPU	FB Memory (GDDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL N13M-GE	Samsung 2500MHz	K4G10325FG-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ1H24BFR-T2C						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 2500MHz	K4G20325FG-HC04						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ2H24MFR-T2C						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

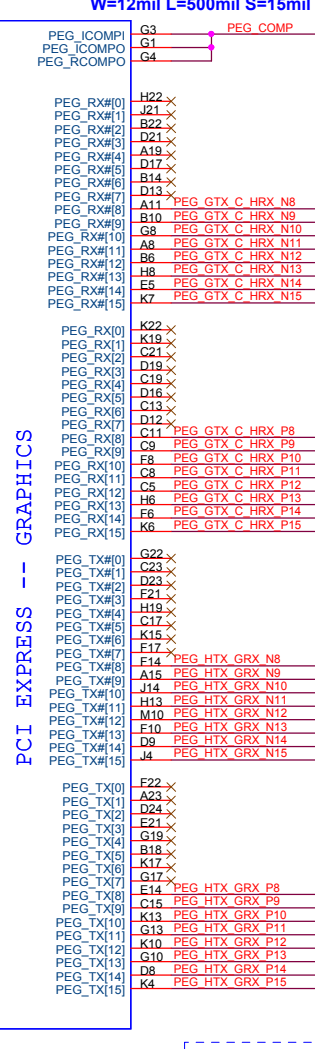
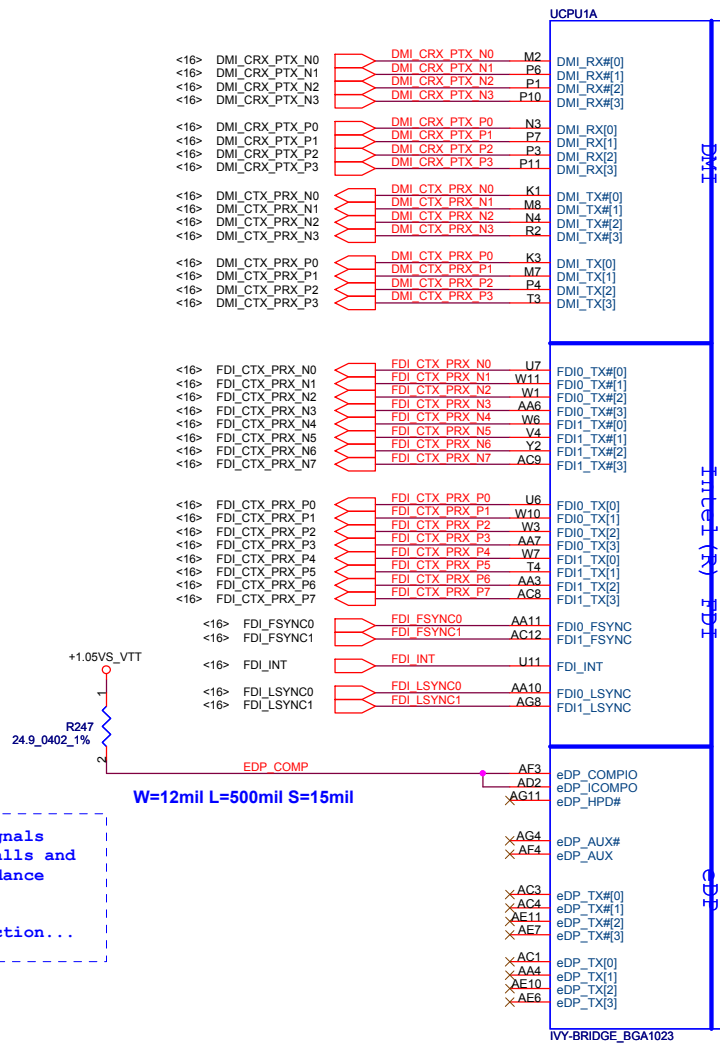


1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

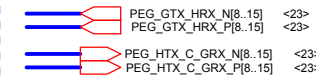


1. all GPU power rails should be turned off within 10ms

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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms  
can't be left floating  
even if disable eDP function...

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

PCH->CPU  
UNCOREPWRGOOD:非CORE外的電OK  
SM\_DRAMPWROK:DRAM power ok  
RESET#:都ok後請CPU做reset

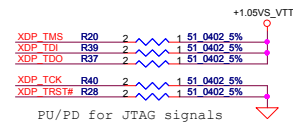
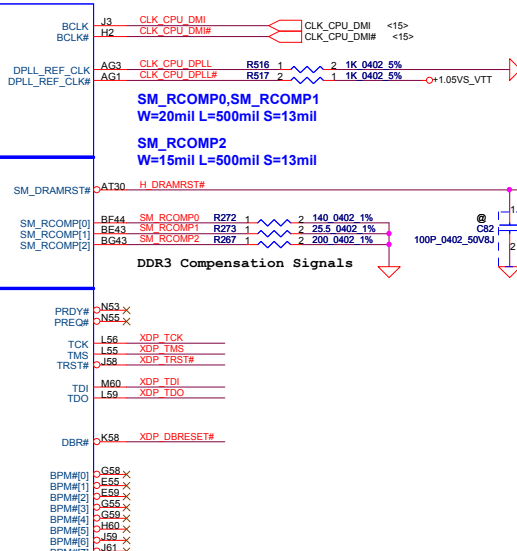
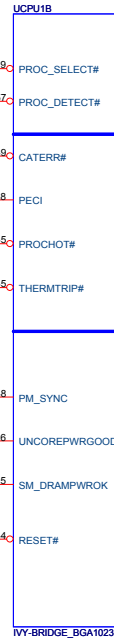
Follow DG 1.5& Tacoma\_Fall2 1.0  
reserve

UNCOREPWRGOOD:非CORE外的電OK

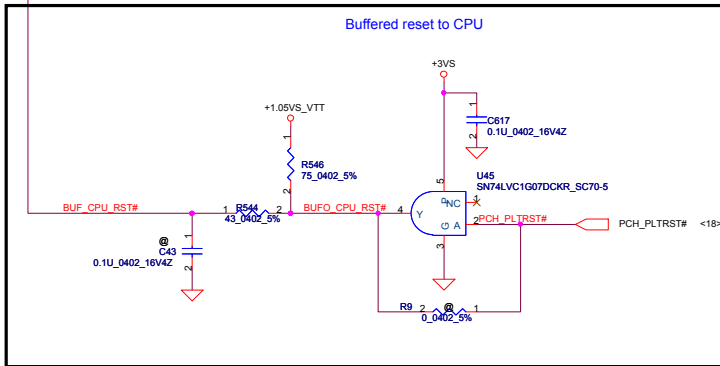
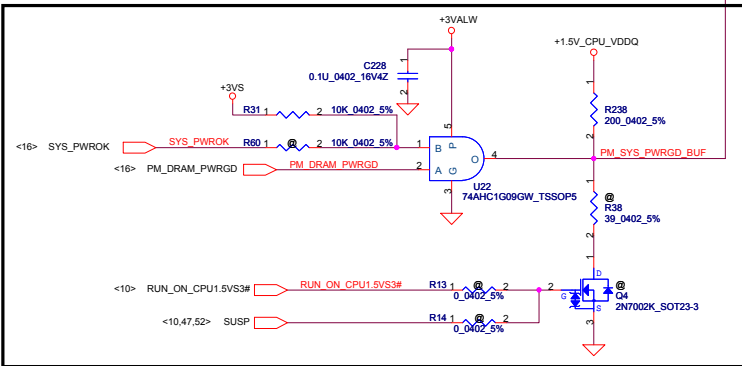
PROC\_SELECT#  
PH VCPLL and connect to PCH DF\_TVS

XBOX 三紅功能

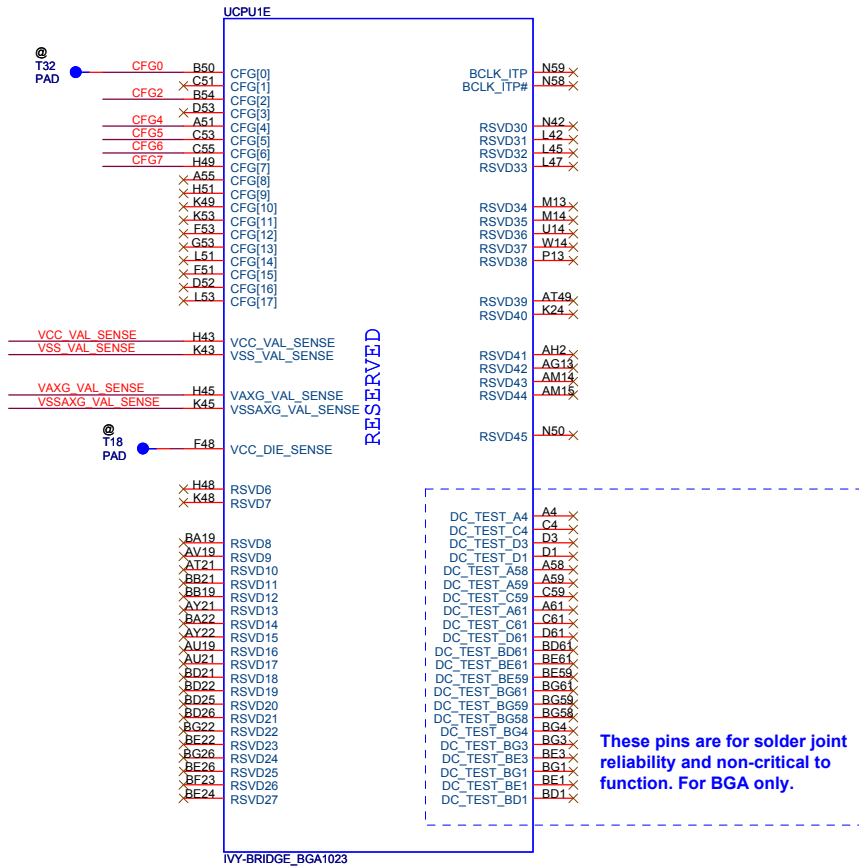
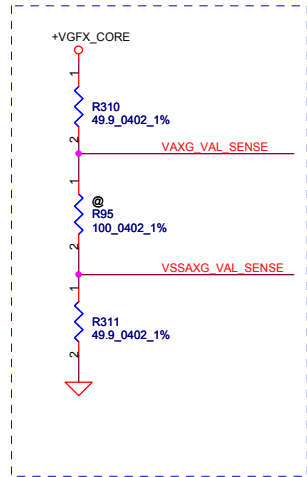
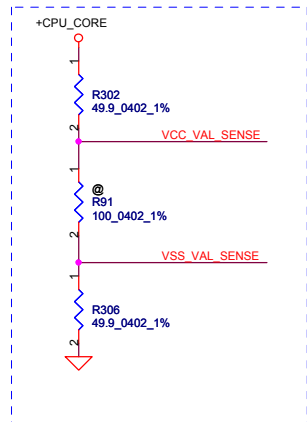
CLOCKS  
THERMAL  
DDR3 MISC  
PWR MANAGEMENT  
JTAG & BPM



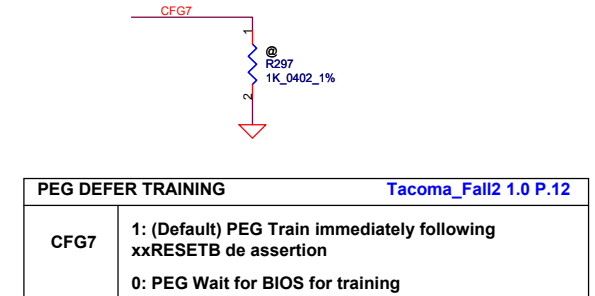
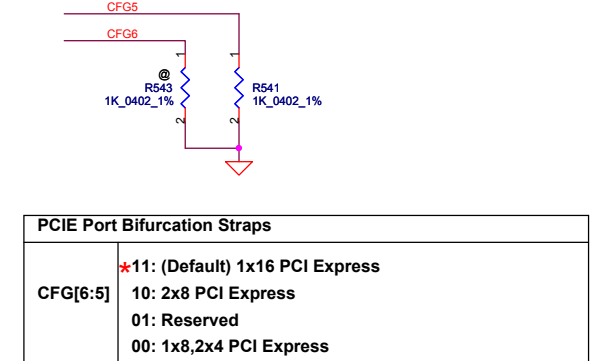
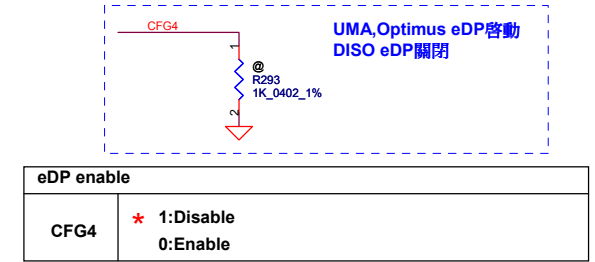
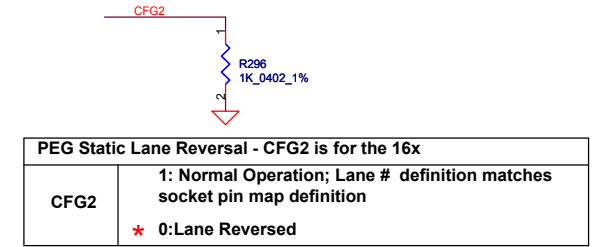
Tacoma\_Fall2 1.0 PH 1K +3VS  
Check list 1.5 PH 1K +3VS  
Debug port DG1.1-1.3 50-5K ohm







## CFG Straps for Processor



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INTEL Recommend VCC  
4\*470uF,12\*22uF(0805) and 35\*2.2uF(0402)  
PD0.8  
CAP at Power side

ULV type  
DC 33A

UCPU1F

## POWER

8.5A

+1.05VS\_VTT

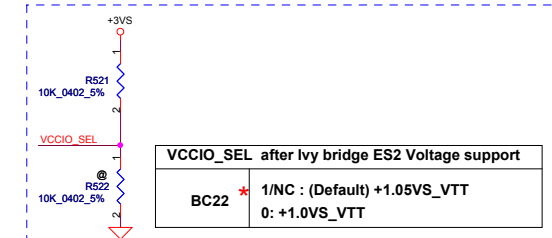
VCCIO[1] AF46  
VCCIO[3] AG48  
VCCIO[5] AG50  
VCCIO[6] AG51  
VCCIO[7] AJ17  
VCCIO[8] AJ21  
VCCIO[9] AJ25  
VCCIO[10] AJ47  
VCCIO[11] AK50  
VCCIO[12] AK51  
VCCIO[13] AL14  
VCCIO[14] AL15  
VCCIO[15] AL16  
VCCIO[16] AL20  
VCCIO[17] AL22  
VCCIO[18] AL26  
VCCIO[19] AL45  
VCCIO[20] AL48  
VCCIO[21] AM16  
VCCIO[22] AM17  
VCCIO[23] AM21  
VCCIO[24] AM43  
VCCIO[25] AM47  
VCCIO[26] AN20  
VCCIO[27] AN42  
VCCIO[28] AN45  
VCCIO[29] AN48

For DDR

INTEL Recommend VCCIO  
2\*330uF,10\*10uF(0603) and 26\*1uF(0402)  
PD0.8  
CAP at Power side

VCCIO[30] AA14  
VCCIO[31] AA15  
VCCIO[32] AB17  
VCCIO[33] AB20  
VCCIO[34] AC13  
VCCIO[35] AD16  
VCCIO[36] AD18  
VCCIO[37] AD21  
VCCIO[38] AE14  
VCCIO[39] AE15  
VCCIO[40] AE16  
VCCIO[41] AE18  
VCCIO[42] AF20  
VCCIO[43] AG15  
VCCIO[44] AG16  
VCCIO[45] AG17  
VCCIO[46] AG21  
VCCIO[47] AJ14  
VCCIO[48] AJ15

For PEG



+1.05VS\_VTT  
W16  
W17

VCCIO\_SEL BC22 VCCIO\_SEL

QUIET  
RAILS

SVID

SENSE  
LINES

+1.05VS\_VTT  
C553  
1U\_0402\_6.3V6K

VCCPQE[1] AM25  
VCCPQE[2] AN22

VIDALERT# A44 H CPU SVIDALRT#  
VIDCLK B43 H CPU SVIDCLK  
VIDSOUT C44 H CPU SVIDDAT

VCC\_SENSE F43 VCCSENSE\_R  
VSS\_SENSE G43 VSSSENSE\_R

VCCIO\_SENSE AN16  
VSSIO\_SENSE AN17

+1.05VS\_VTT  
R531 130\_0402\_5%  
R529 75\_0402\_5%

Place the PU resistors close to CPU

+1.05VS\_VTT  
R528 1 43\_0402\_1%  
R527 1 0\_0402\_5%  
R530 1 2 0\_0402\_5%

+CPU CORE  
R281 100\_0402\_1%  
R288 100\_0402\_1%

VCCSENSE <56>  
VSSSENSE <56>

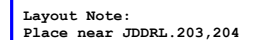
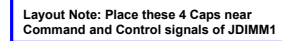
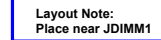
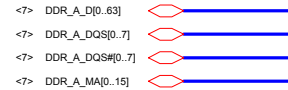
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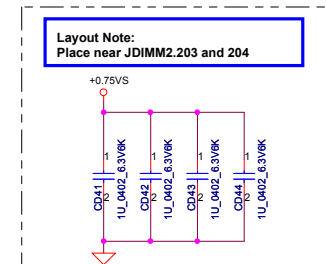
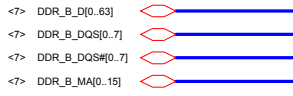
Check list 1.5

Should change to connect form  
power circuit & layout differential  
with VCCIO\_SENSE.



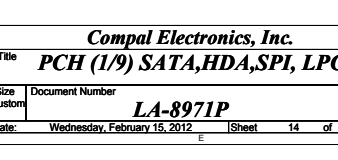
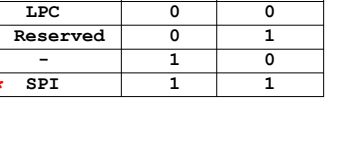
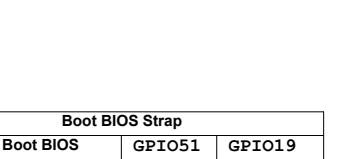
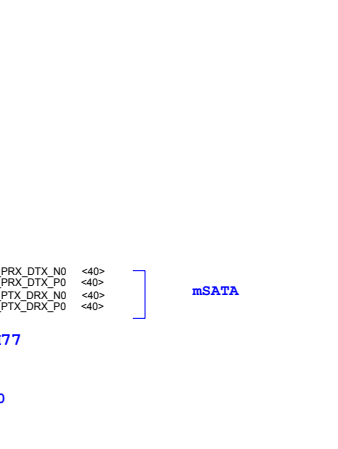
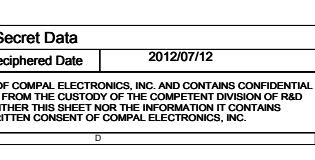
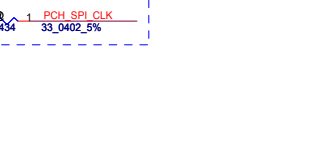
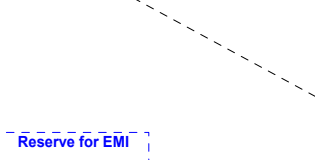
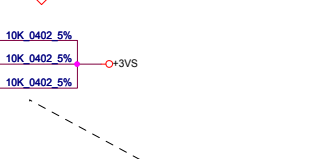
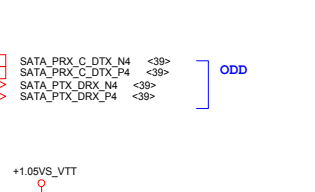
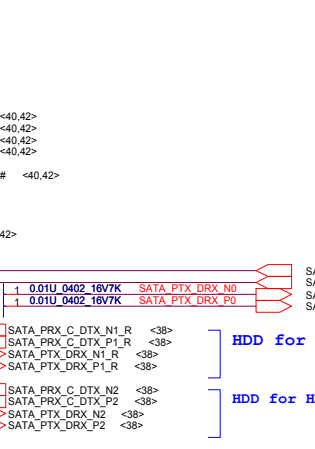
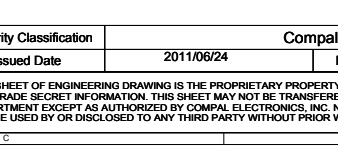
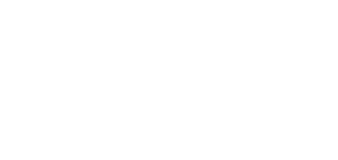
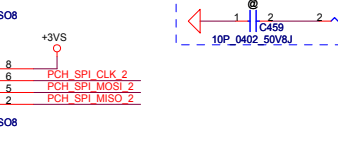
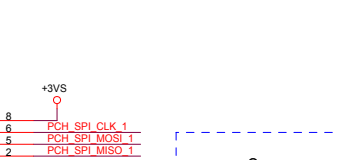
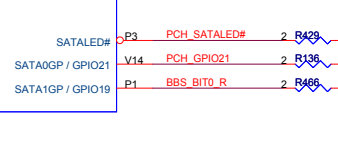
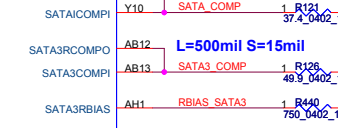
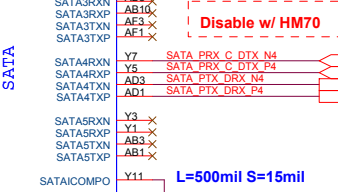
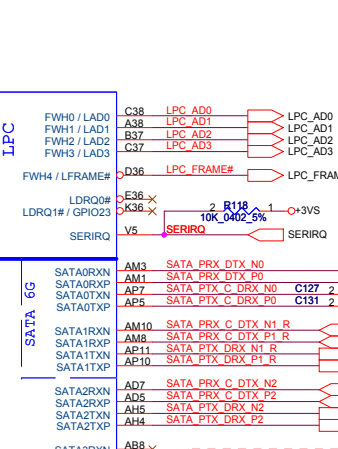
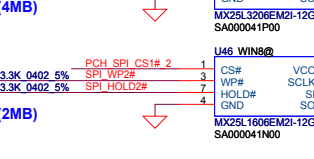
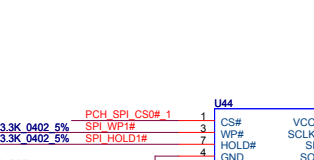
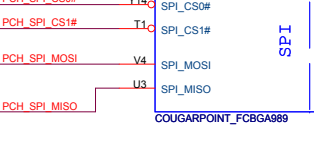
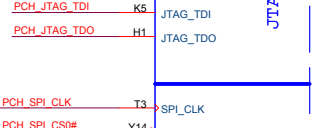
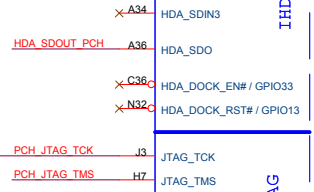
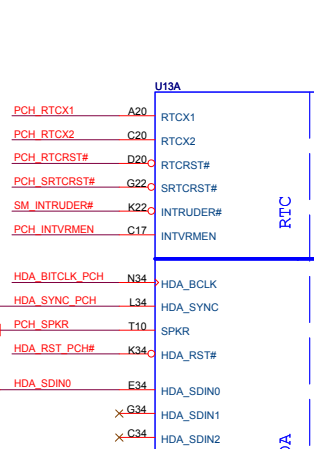
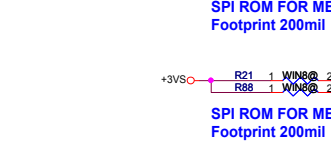
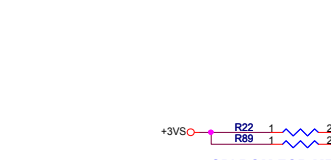
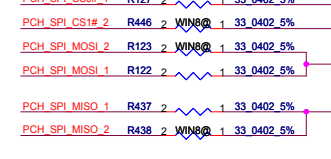
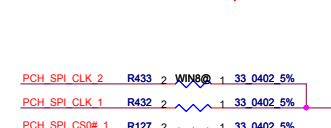
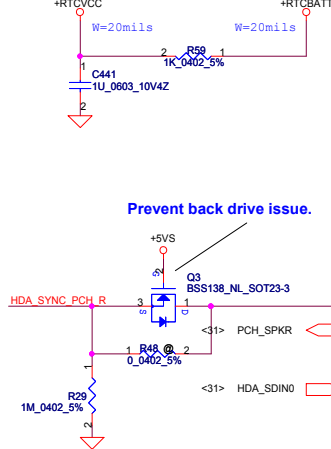
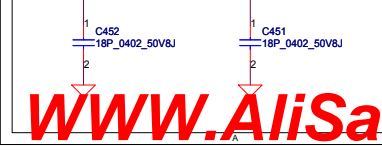
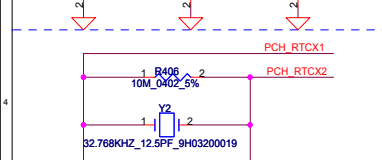
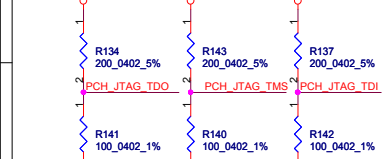
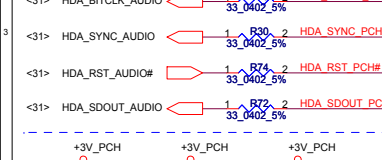
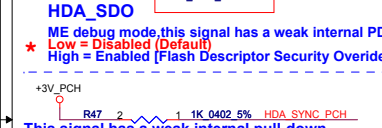
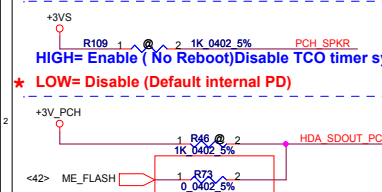
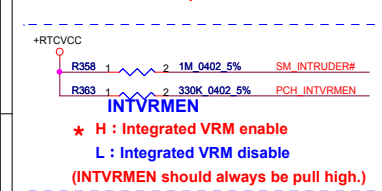
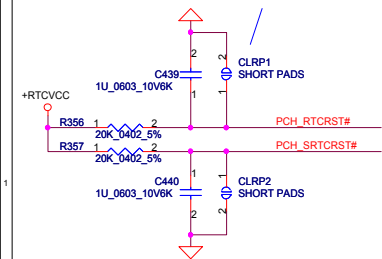




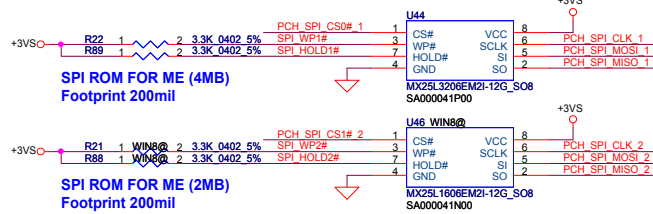


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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	
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Date: Wednesday, February 15, 2012				Sheet 13 of 58	

# CLRP1/2 close RAM door JDIIMM1/2

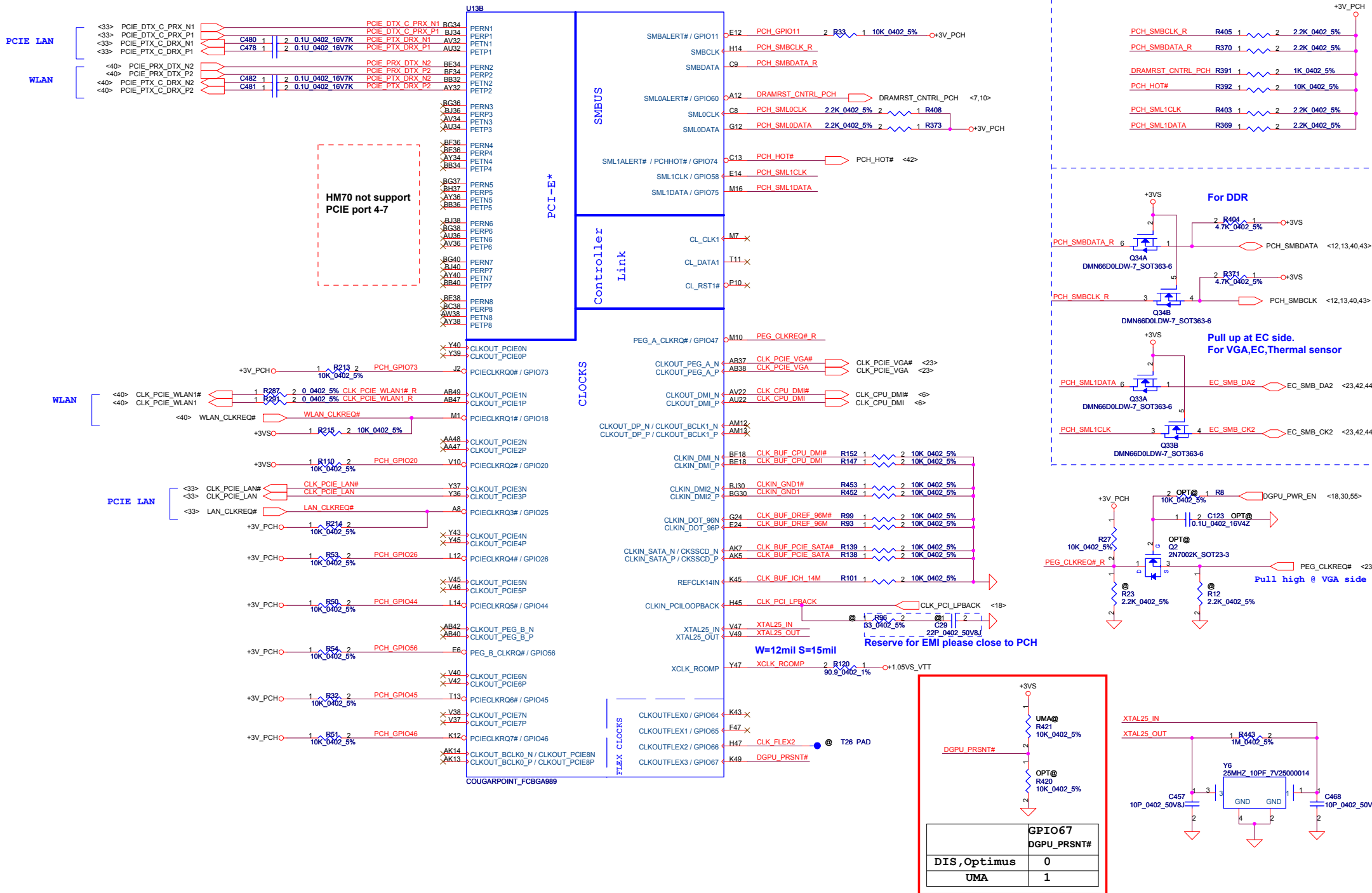


Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1



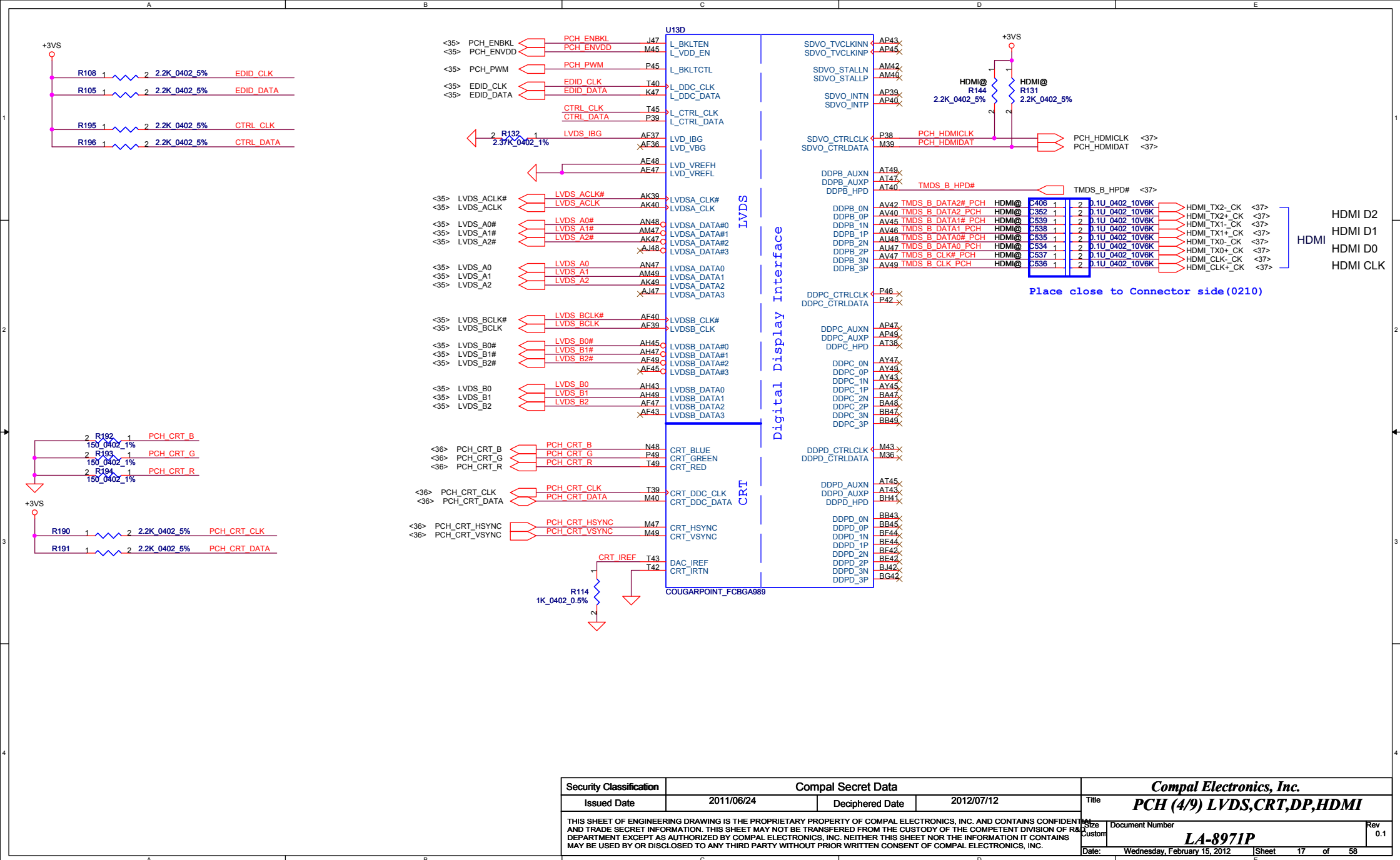
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	PCH (1/9) SATA,HDA,SPI, LPC, XDP
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				LA-8971P	
				Date	Wednesday, February 15, 2012
				Sheet	14 of 58









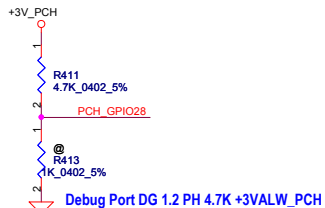




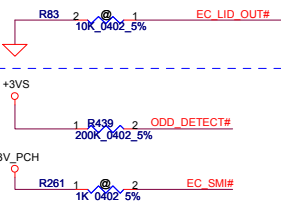
## GPIO28

## On-Die PLL Voltage Regulator

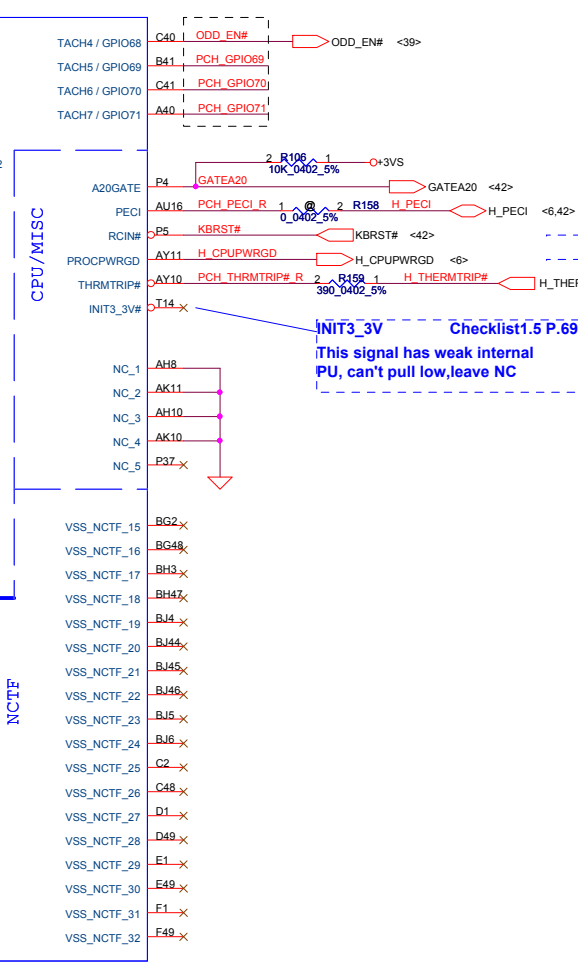
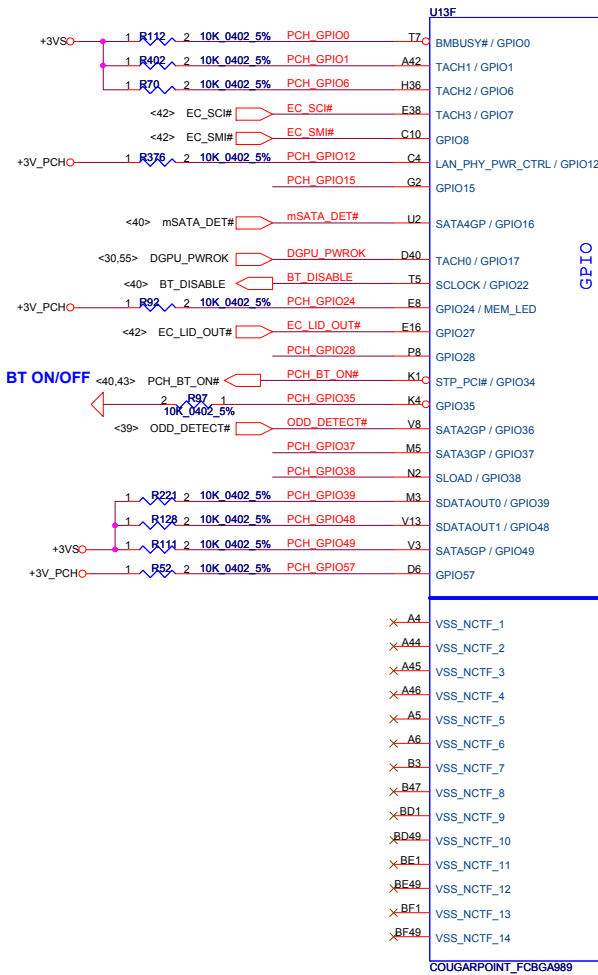
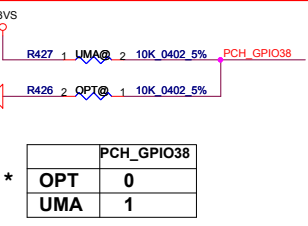
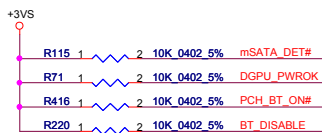
This signal has a weak internal pull up  
★ H : On-Die PLL voltage regulator enable  
L : On-Die PLL Voltage Regulator disable



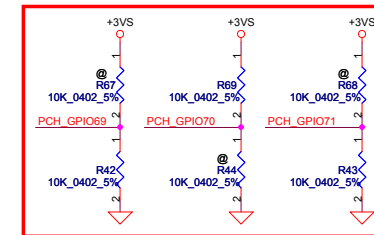
Deep S4,S5 wake event signal  
RTC alarm,Power BTN,GPIO27  
PCH\_GPIO27 (Have internal Pull-High)  
Deep S4,S5 wake event signal



SATA2GP/GPIO36 & SATA3GP/GPIO37  
Sampled at Rising edge of PWROK.  
Weak internal pull-down.  
(weak internal pull-down is disabled  
after PLTRST# de-asserts)  
NOTE: This signal should NOT be  
pulled high when strap is sampled



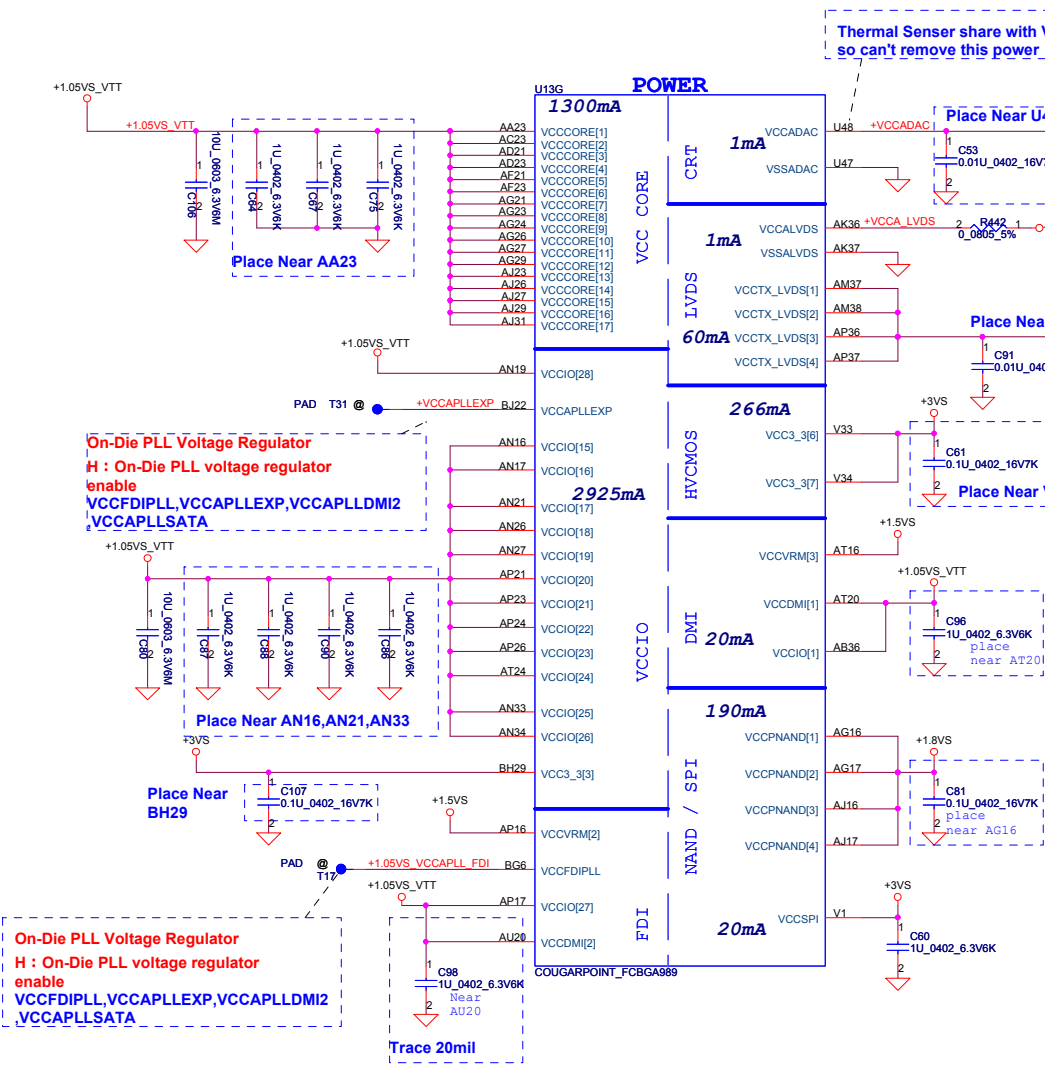
Project ID	GPIO70		
★U510	1		



CTRL+ALT+DEL  
non CPU power ok  
130c shut down

INIT3\_3V  
This signal has weak internal  
PU, can't pull low,leave NC

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I/O Buffer Voltage

Internal PLL and VRM(+1.5VS)

DMI buffer logic

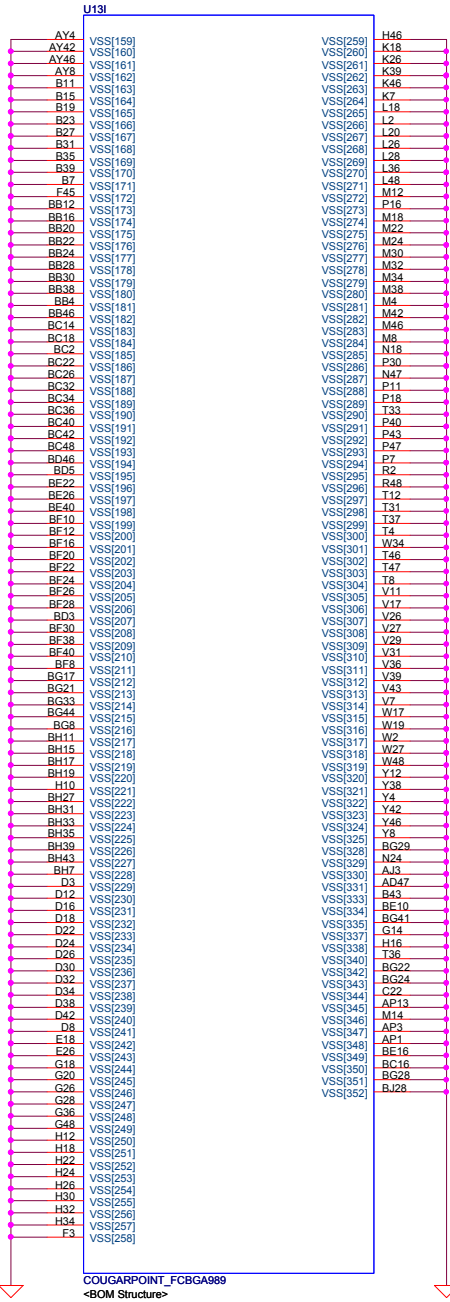
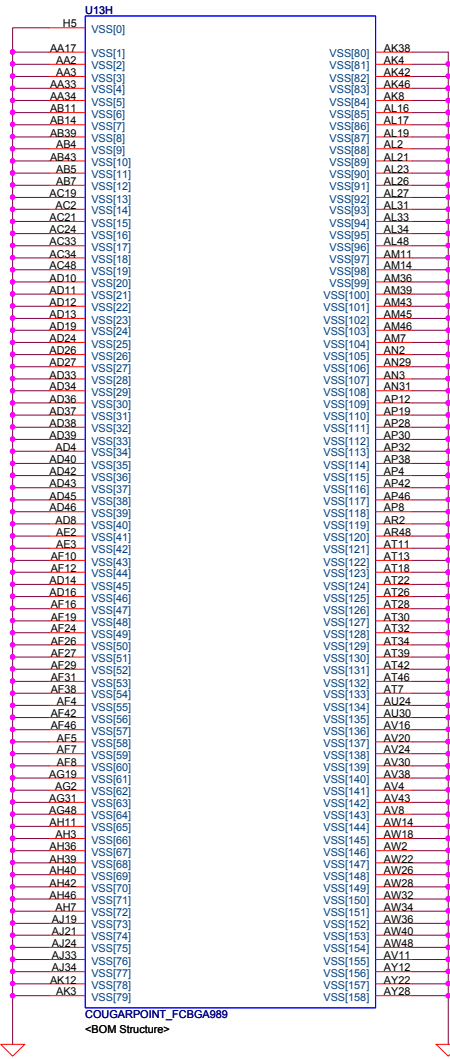
Core Well I/O Buffer

VccDFTerm should PH +1.8VS or +3VS

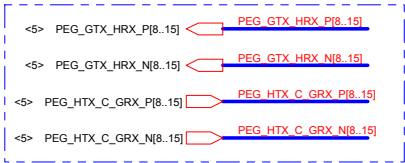
For SPI control logi

PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)



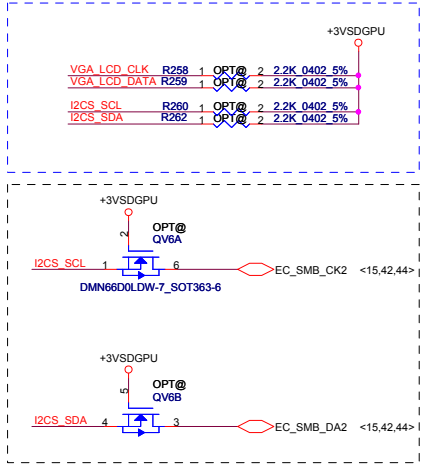
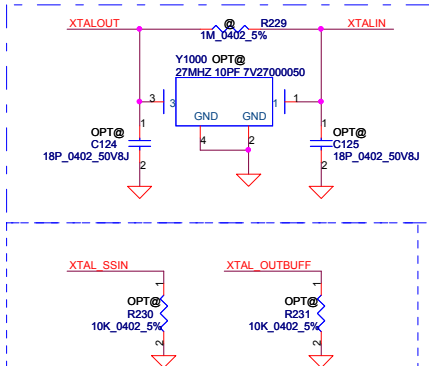
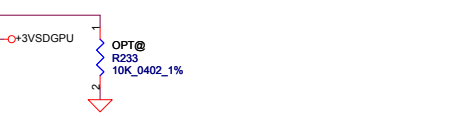
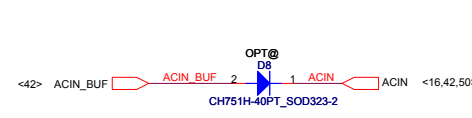
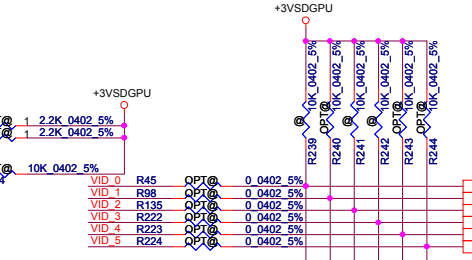
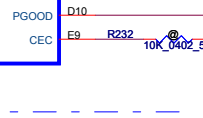
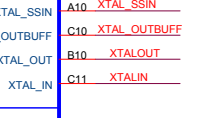
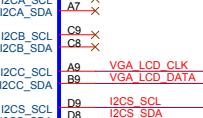
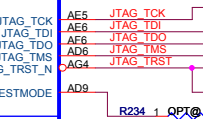
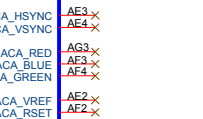
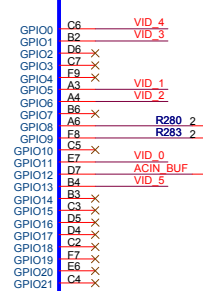
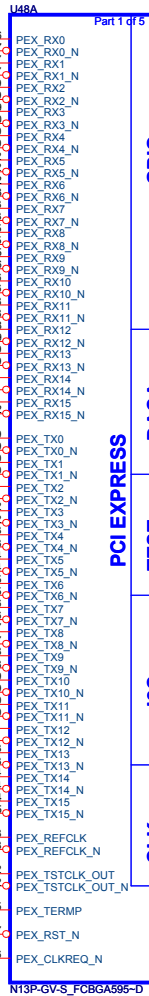
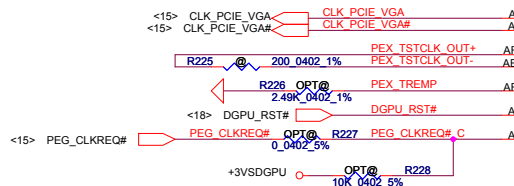






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PEG HTX\_C\_GRX\_P13 AG9 PEX\_RX2  
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PEG HTX\_C\_GRX\_P12 AE10 PEX\_RX3  
PEG HTX\_C\_GRX\_N12 AE11 PEX\_RX3\_N  
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PEG GTX\_HRX\_P0 AC24 PEX\_TX15  
PEG GTX\_HRX\_N0 AB25 PEX\_TX15\_N



GPIO	I/O	USAGE
GPIO0	O	GPU Core VID4
GPIO1	O	GPU Core VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU Core VID1
GPIO6	O	GPU Core VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU Core VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU Core VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

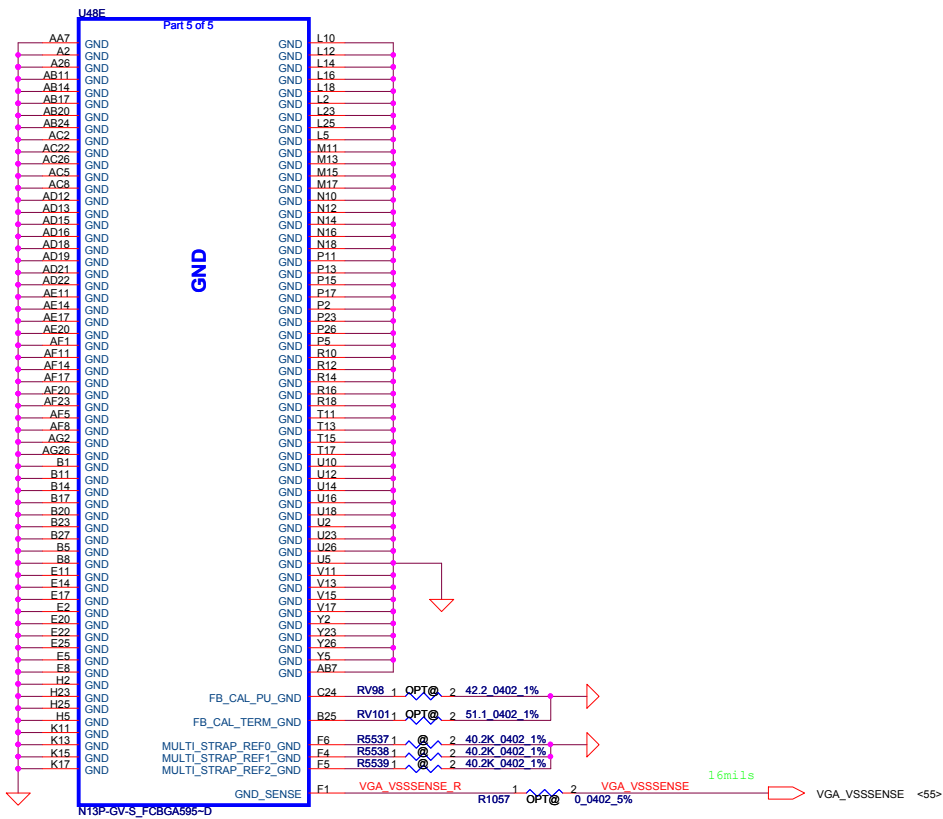
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Document Number	N13M-GS 1/7
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				Date: Wednesday, February 15, 2012	Sheet 23 of 58





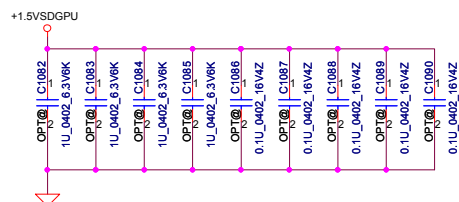
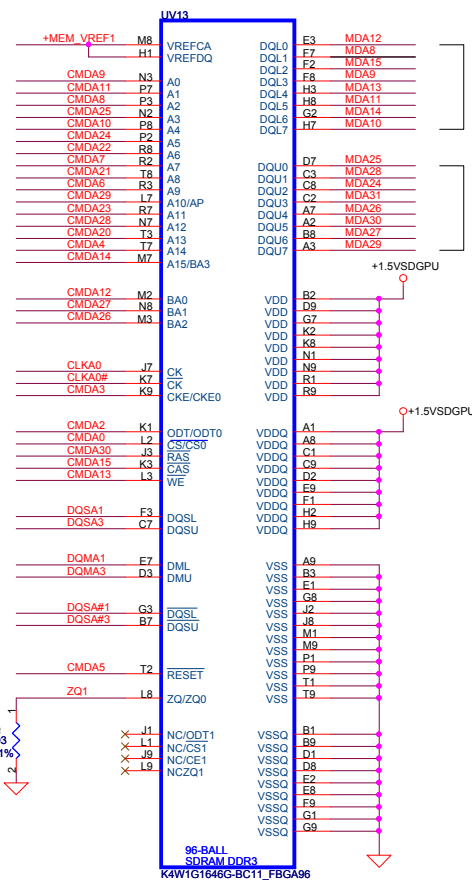
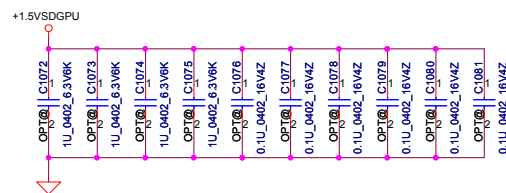
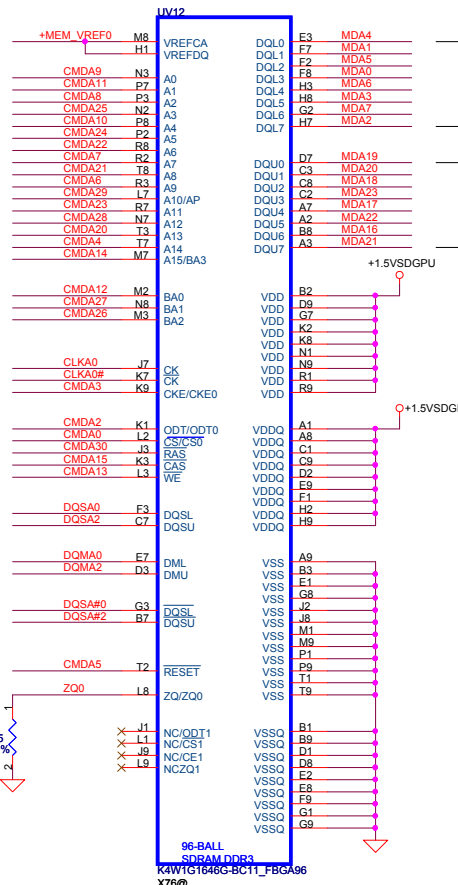
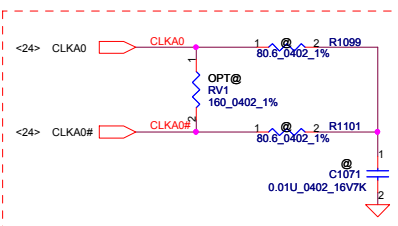






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				Date:	Wednesday, February 15, 2012	Sheet 27 of 58

**128Mx16 DDR3 \*4==>1GB**



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

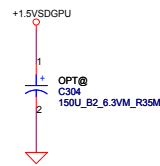
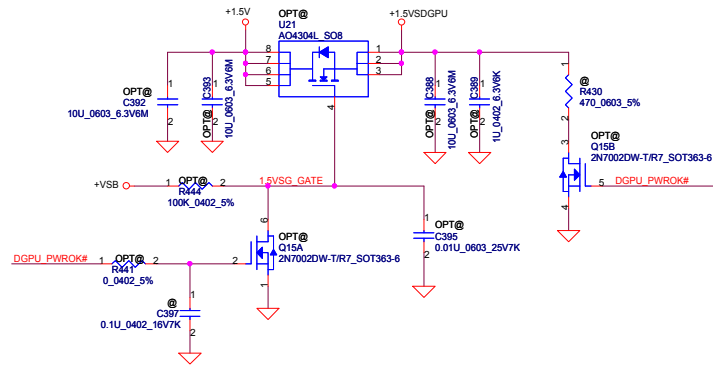
CMDA2	RV1121	OPT@	2	10K	0402	5%
CMDA3	RV1131	OPT@	2	10K	0402	5%
CMDA5	RV1151	OPT@	2	10K	0402	5%
CMDA18	RV1161	OPT@	2	10K	0402	5%
CMDA19	RV1171	OPT@	2	10K	0402	5%

Samsung :  
Hynix :

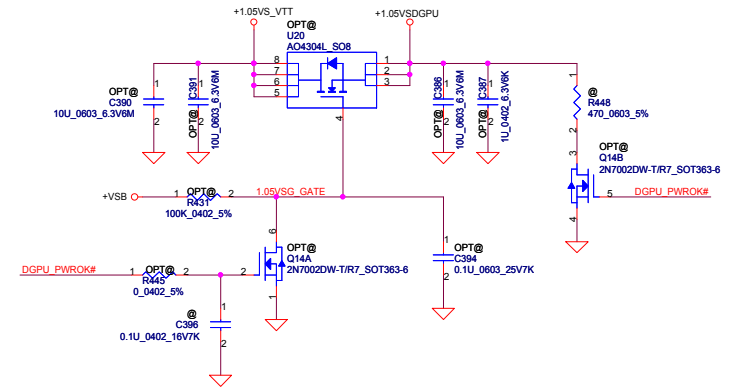
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	N13M-GS 6/7	
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				Custom	LA-8971P	0.1
Date:				Wednesday, February 15, 2012	Sheet	28 of 58

**128Mx16 DDR3 \*4==>1GB**

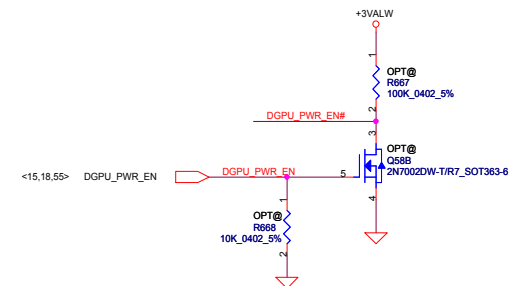
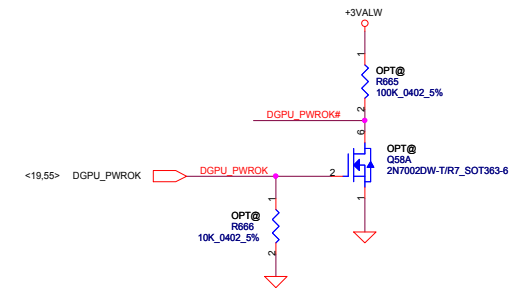
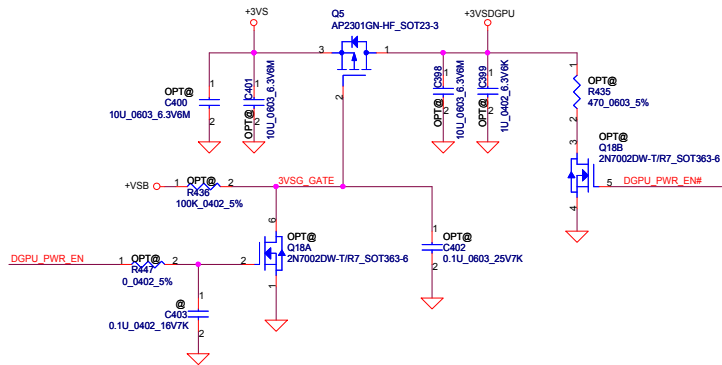
**+1.5V to +1.5VSDGPU**



**+VCCP to +1.05VSDGPU**

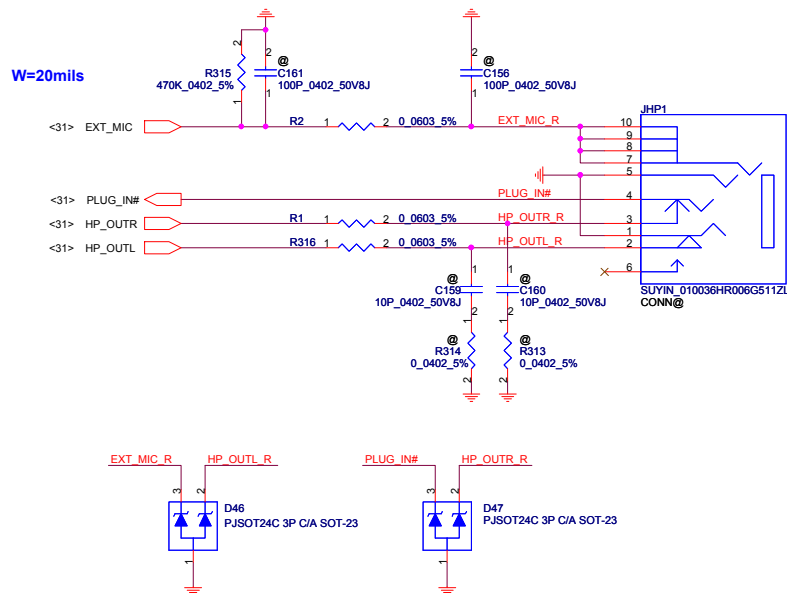


**+3VS to +3VSDGPU**



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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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				Custom	0.3
Date: Wednesday, February 15, 2012				Sheet	30 of 58

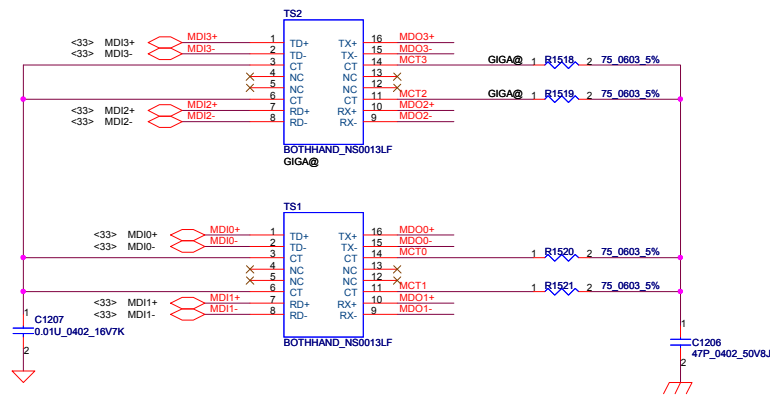




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				LA-8971P	0.1
				Date: Wednesday, February 15, 2012	Sheet 32 of 58

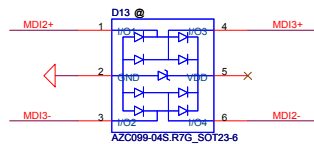
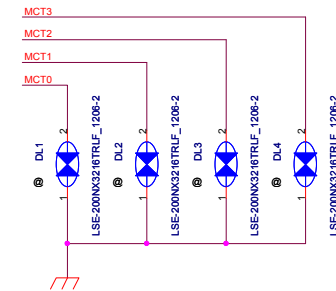


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				Custom	LA-8971P	0.1	
				Date:	Wednesday, February 15, 2012	Sheet	33 of 58

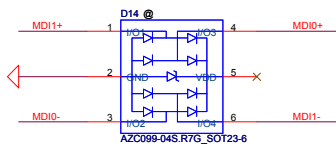


Reserve gas tube for EMI go rural solution

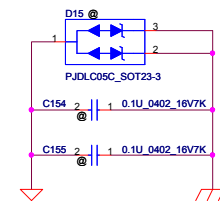
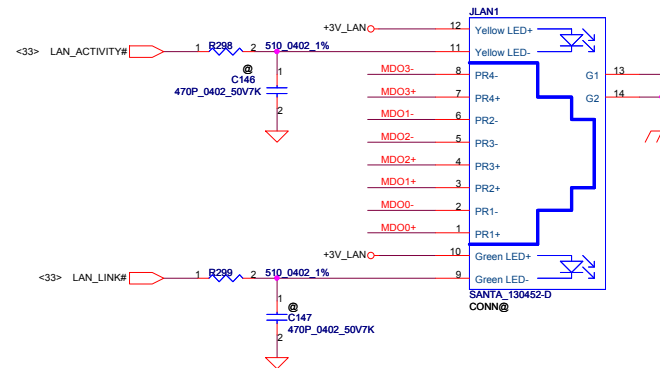
Place Close to TS1, TS2



Place Close to TS2

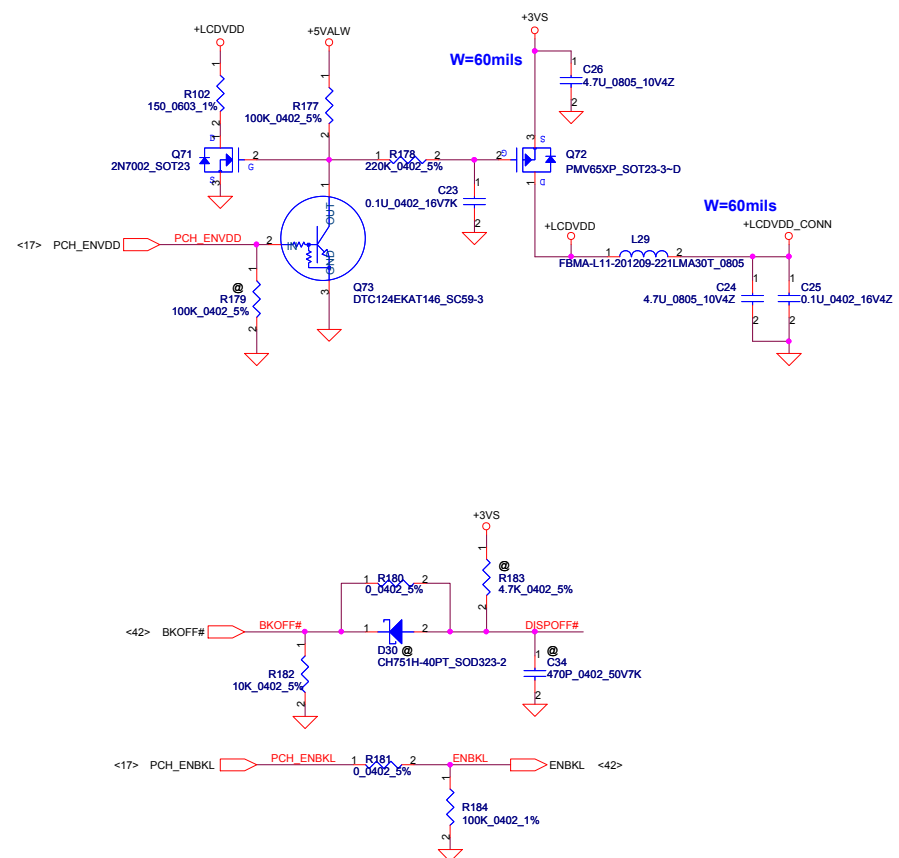


Place Close to TS1

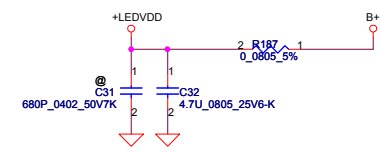
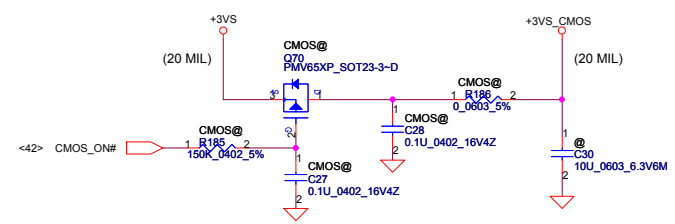


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				Date	Wednesday, February 15, 2012
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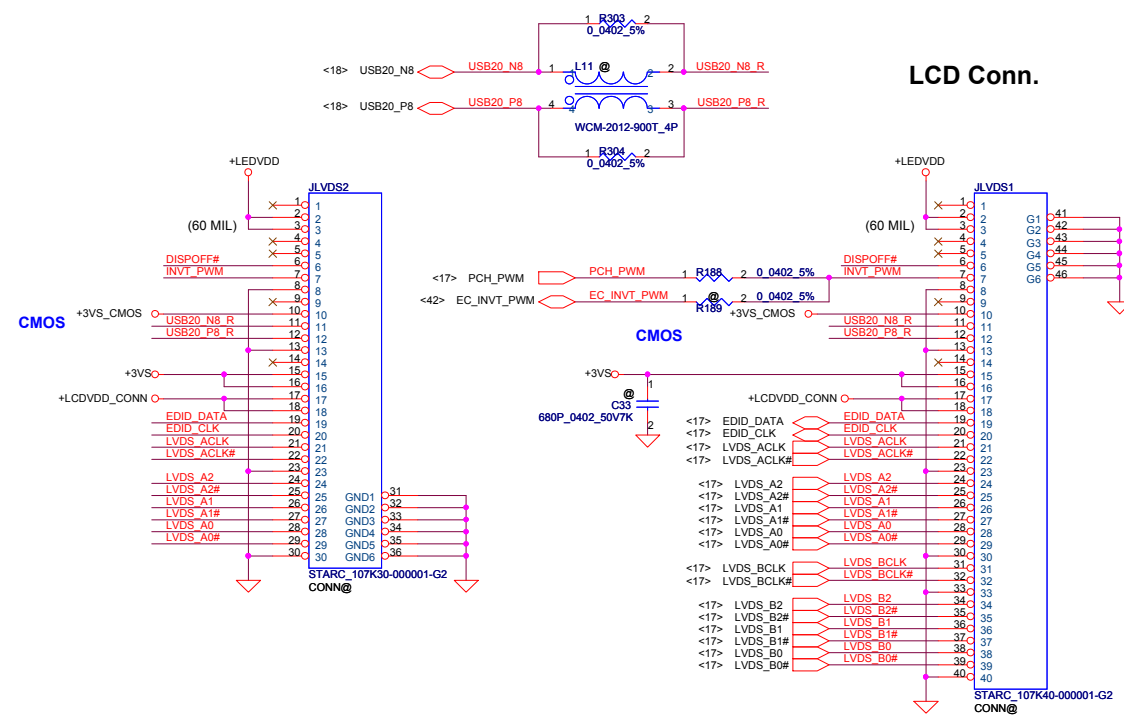
LCD POWER CIRCUIT



CMOS Camera

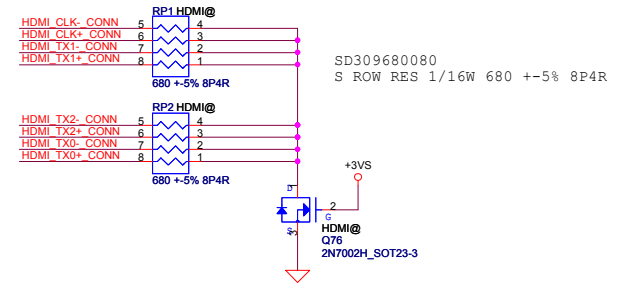
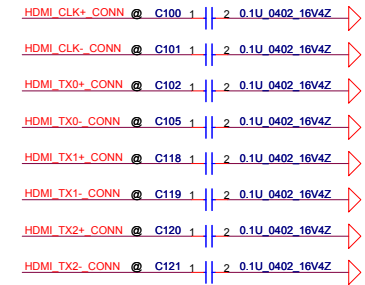
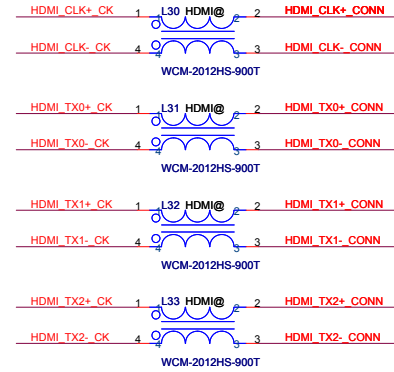
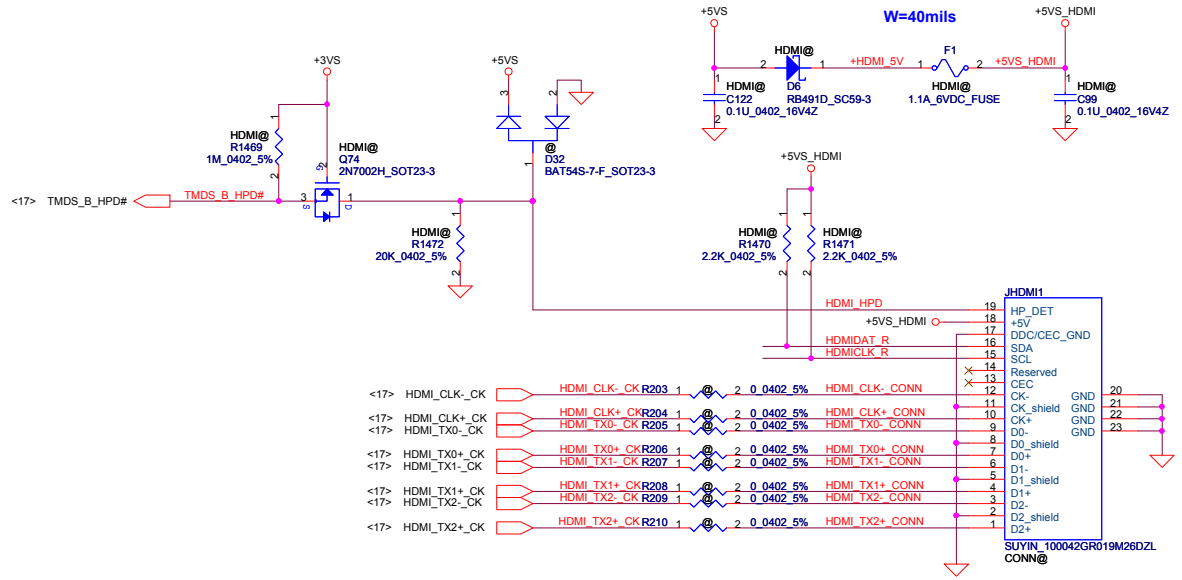
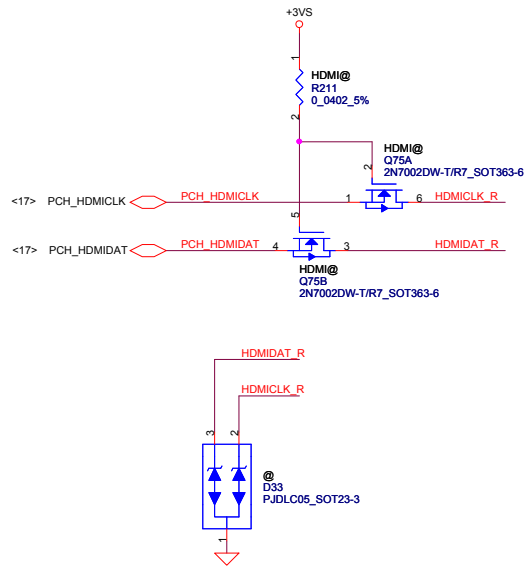


LCD Conn.



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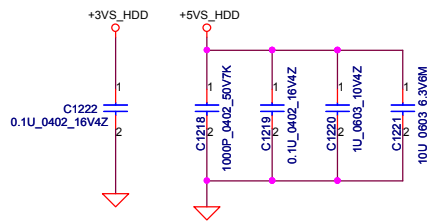
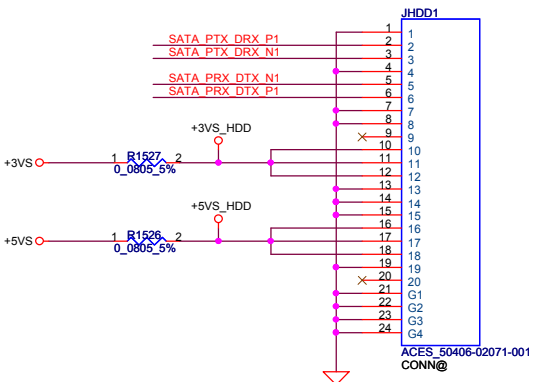
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						Document Number		LA-8971P		Rev 0.1	
						Date: Wednesday, February 15, 2012		Sheet 37 of 58			

SATA HDD Conn.

<14>	SATA_PRX_C_DTX_N1_R	SATA PRX C DTX N1 R	HM77@ C134	2	1	0.01U_0402_16V7K	SATA PRX DTX N1
<14>	SATA_PRX_C_DTX_P1_R	SATA PRX C DTX P1 R	HM77@ C135	2	1	0.01U_0402_16V7K	SATA PRX DTX P1
<14>	SATA_PT_X_DRX_N1_R	SATA PTX DRX N1 R	HM77@ C139	2	1	0.01U_0402_16V7K	SATA PTX DRX N1
<14>	SATA_PT_X_DRX_P1_R	SATA PTX DRX P1 R	HM77@ C140	2	1	0.01U_0402_16V7K	SATA PTX DRX P1

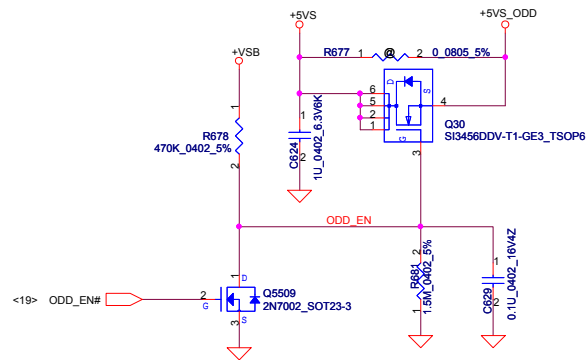
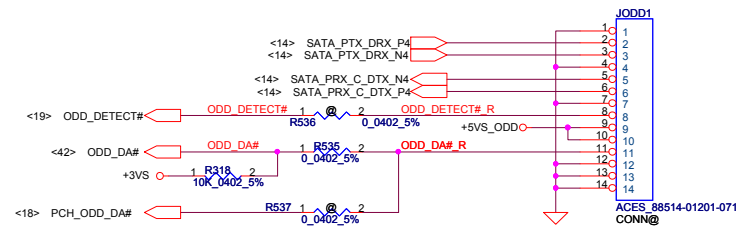
  

<14>	SATA_PRX_C_DTX_N2	SATA PRX C DTX N2	HM70@ C132	2	1	0.01U_0402_16V7K	SATA PRX DTX N1
<14>	SATA_PRX_C_DTX_P2	SATA PRX C DTX P2	HM70@ C133	2	1	0.01U_0402_16V7K	SATA PRX DTX P1
<14>	SATA_PT_X_DRX_N2	SATA PTX DRX N2	HM70@ C138	2	1	0.01U_0402_16V7K	SATA PTX DRX N1
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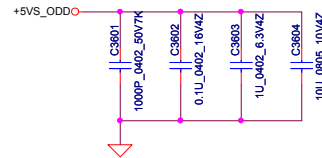


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**SATA ODD FFC CONN.**

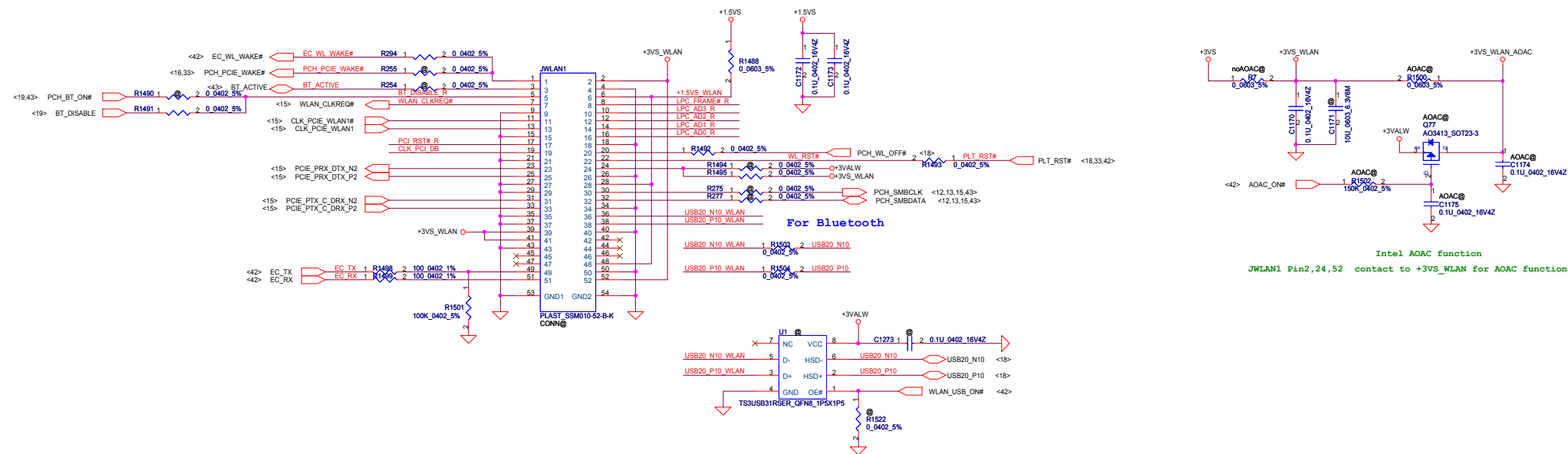


Place caps. near ODD CONN.

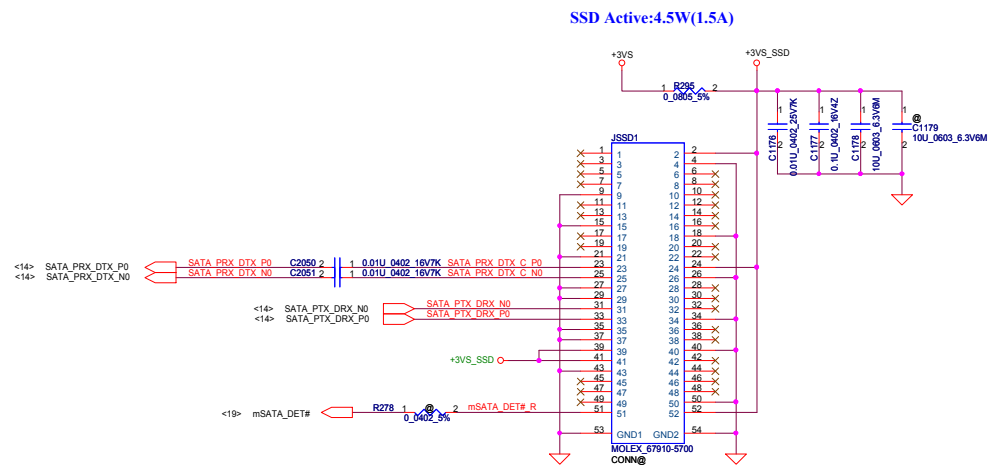


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				Custom	0.3	
				Date: Wednesday, February 15, 2012	Sheet 39	of 58

### Mini-Express Card for WLAN with BT(Half)

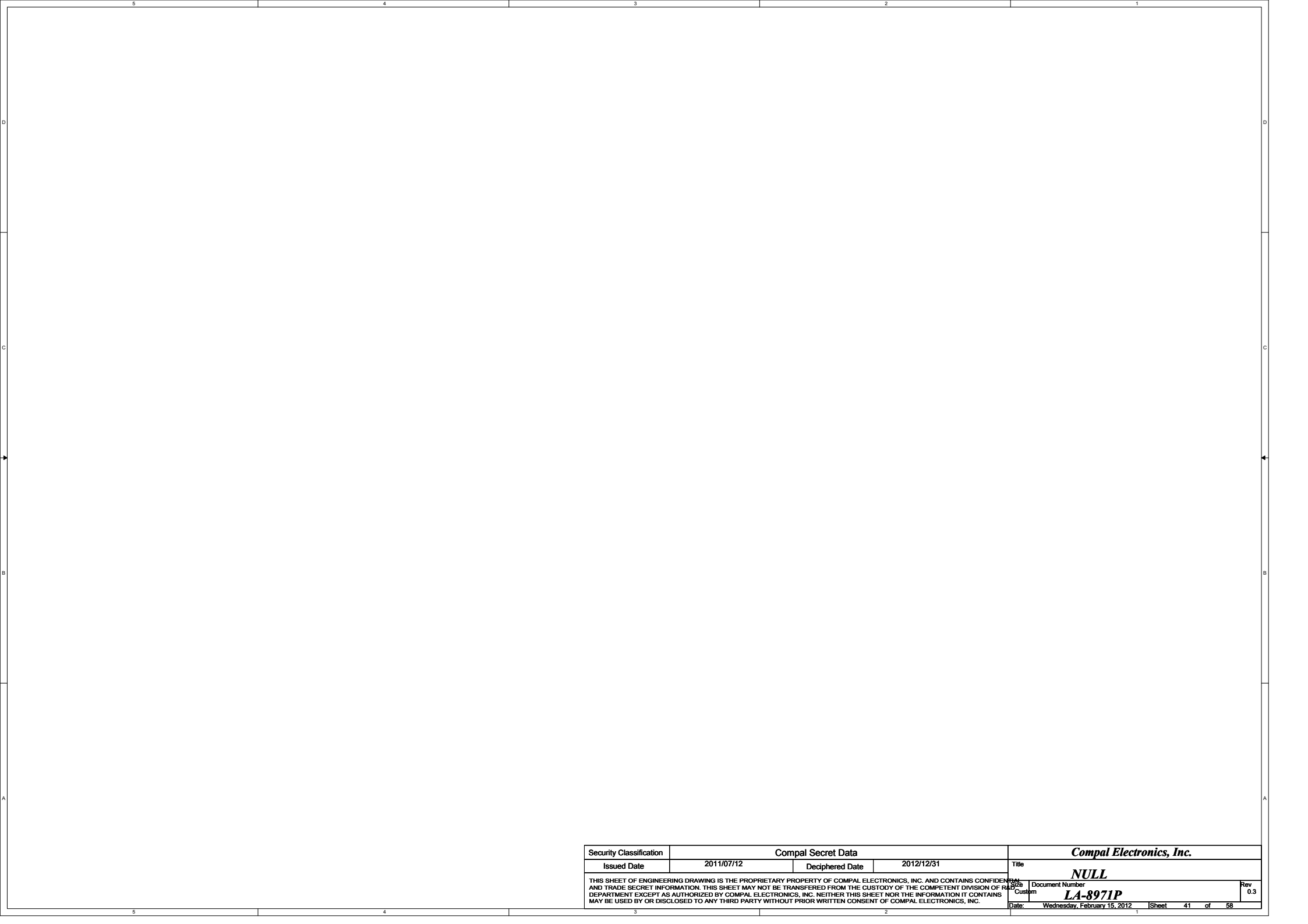


### Mini-Express Card for SSD(Full)



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Issued Date		2011/07/21	Deciphered Date	2012/12/31	Title
					W/L & m-SATA Card
				Size	Document Number
					LA-8971P
				Date:	Wednesday, February 15, 2012
				Sheet	40 of 58
					Rev 0.1
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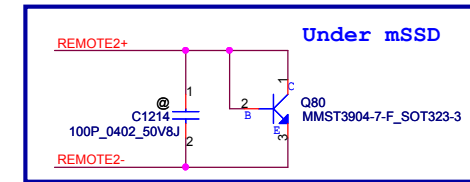
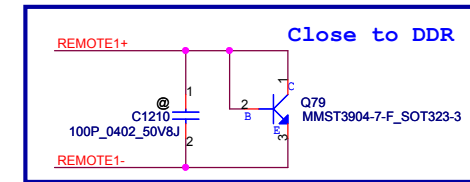
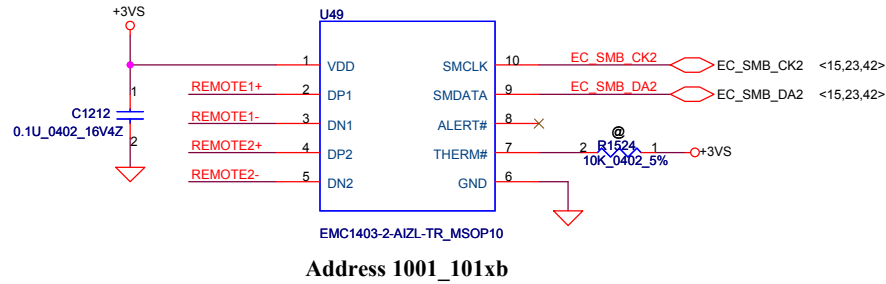
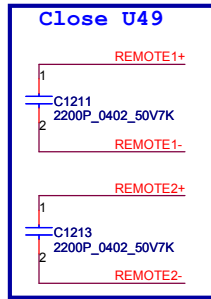


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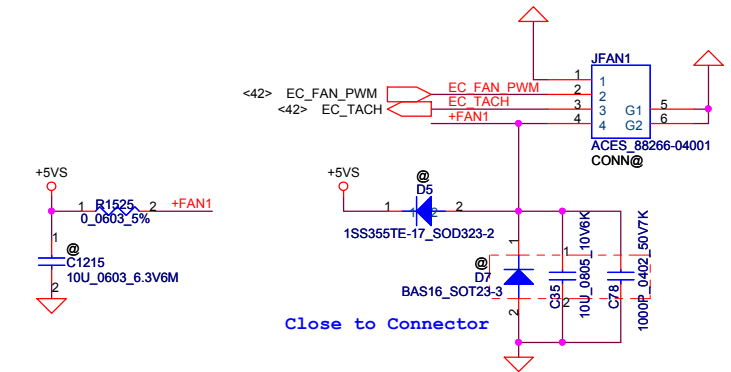


## SMSC thermal sensor placed near by VRAM



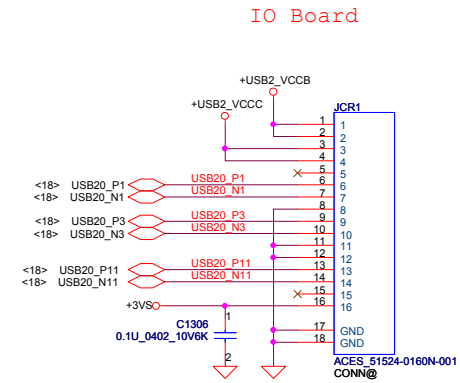
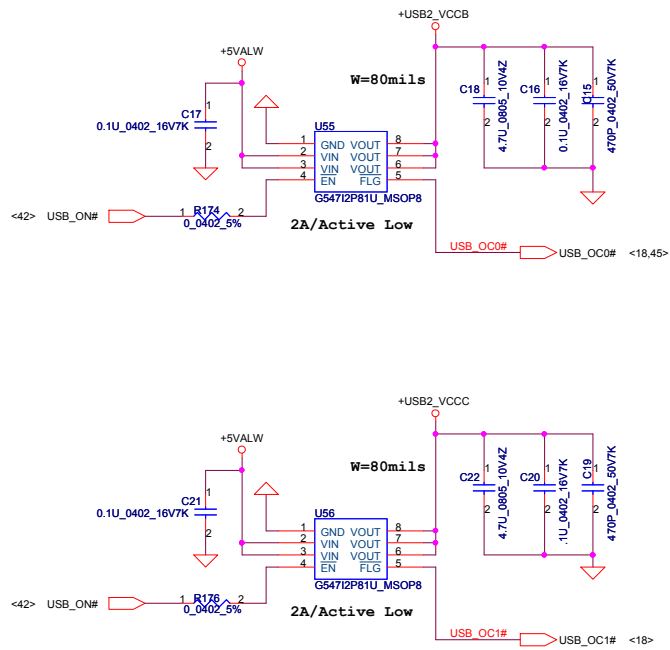
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Trace length:<8"

## FAN Conn

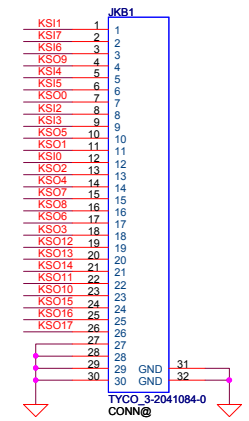
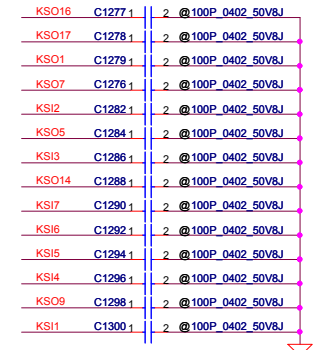
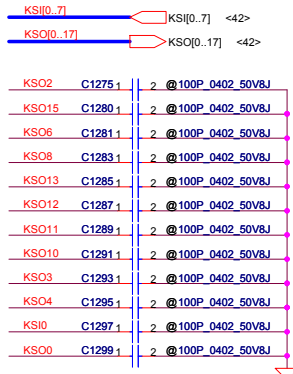
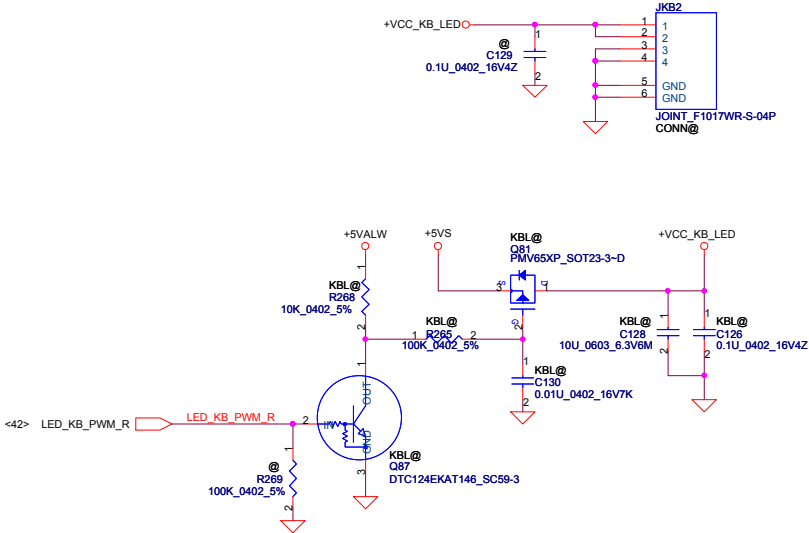


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				Date: Wednesday, February 15, 2012	Sheet 44 of 58

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <i>USB3.0 Left Side</i>		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title		
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				Custom	LA-8971P	0.1
				Date:	Wednesday, February 15, 2012	Sheet 45 of 58



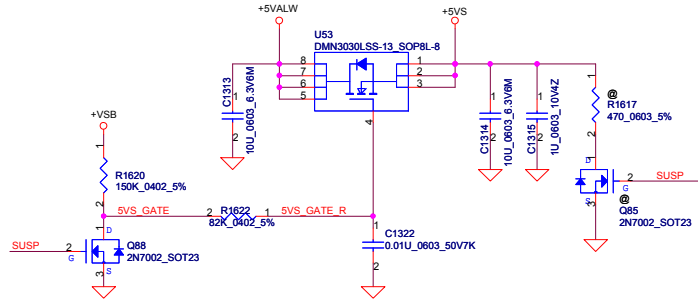
# KB BackLight Connector



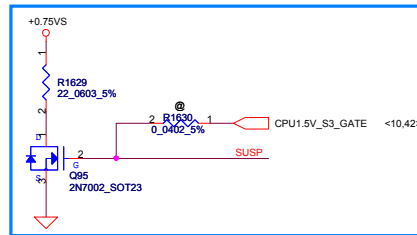
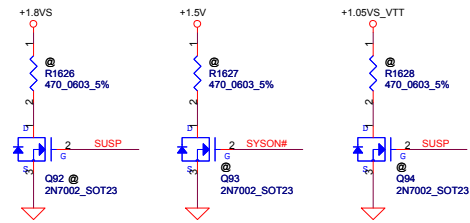
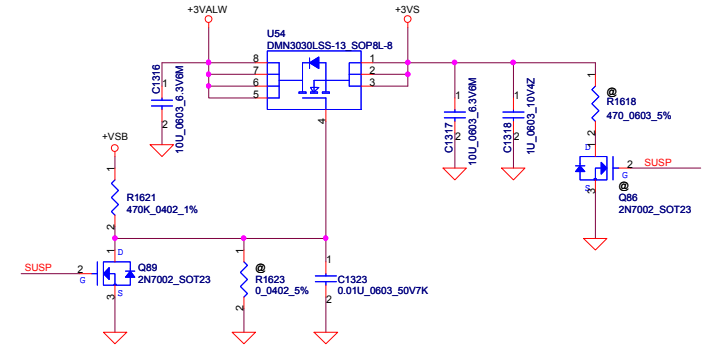
WWW.AliSaler.Com

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Date		Thursday, February 16, 2012		Sheet		46 of 58		LA-8971P			
								Rev 0.1			

### +5VALW TO +5VS

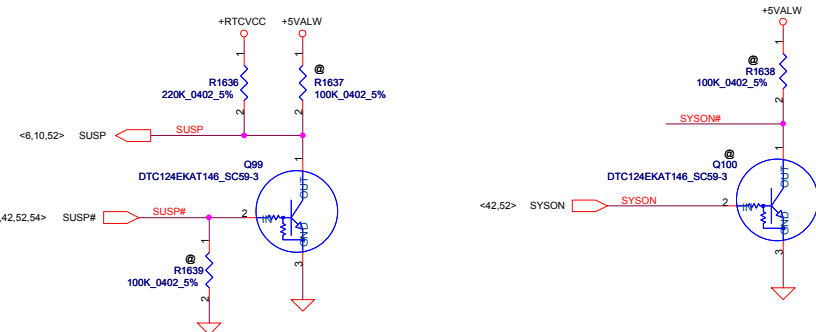
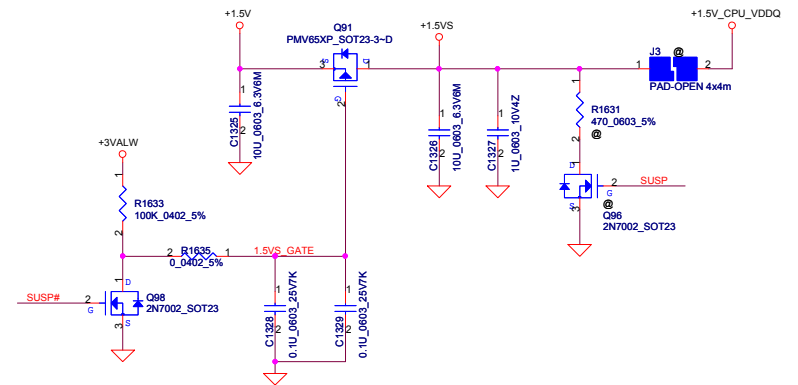


### +3VALW TO +3VS



For Intel S3 Power Reduction.

### +1.5V to +1.5VS



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				DC Interface			
				Size	Document Number	LA-8971P	
Custom						0.1	
Date:				Wednesday, February 15, 2012			
				Sheet		47 of 58	





ADP\_I need to write Charge Options Register (0x12H)=> bit6=1

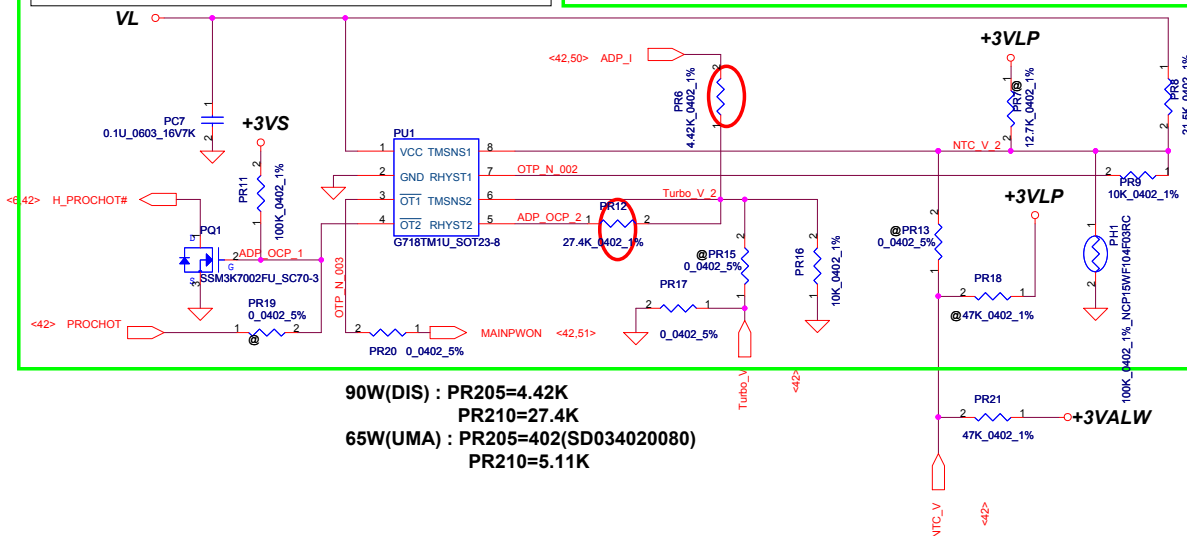
0: IOUT is the 20x current amplifier output <default @ POR>

1: IOUT is the 40x current amplifier output

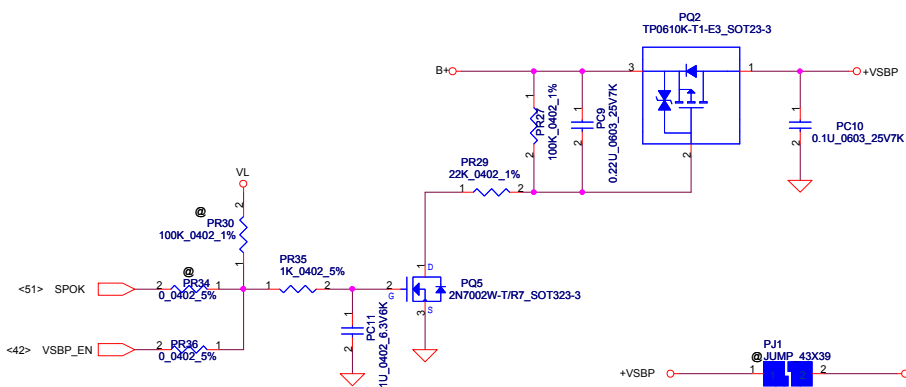
PH1 under CPU bottom side :  
CPU thermal protection at 93 +/-3 degree C  
Recovery at 56 +/-3 degree C

For KB930 --> Keep PU201 circuit  
(Vth = 1.25V)

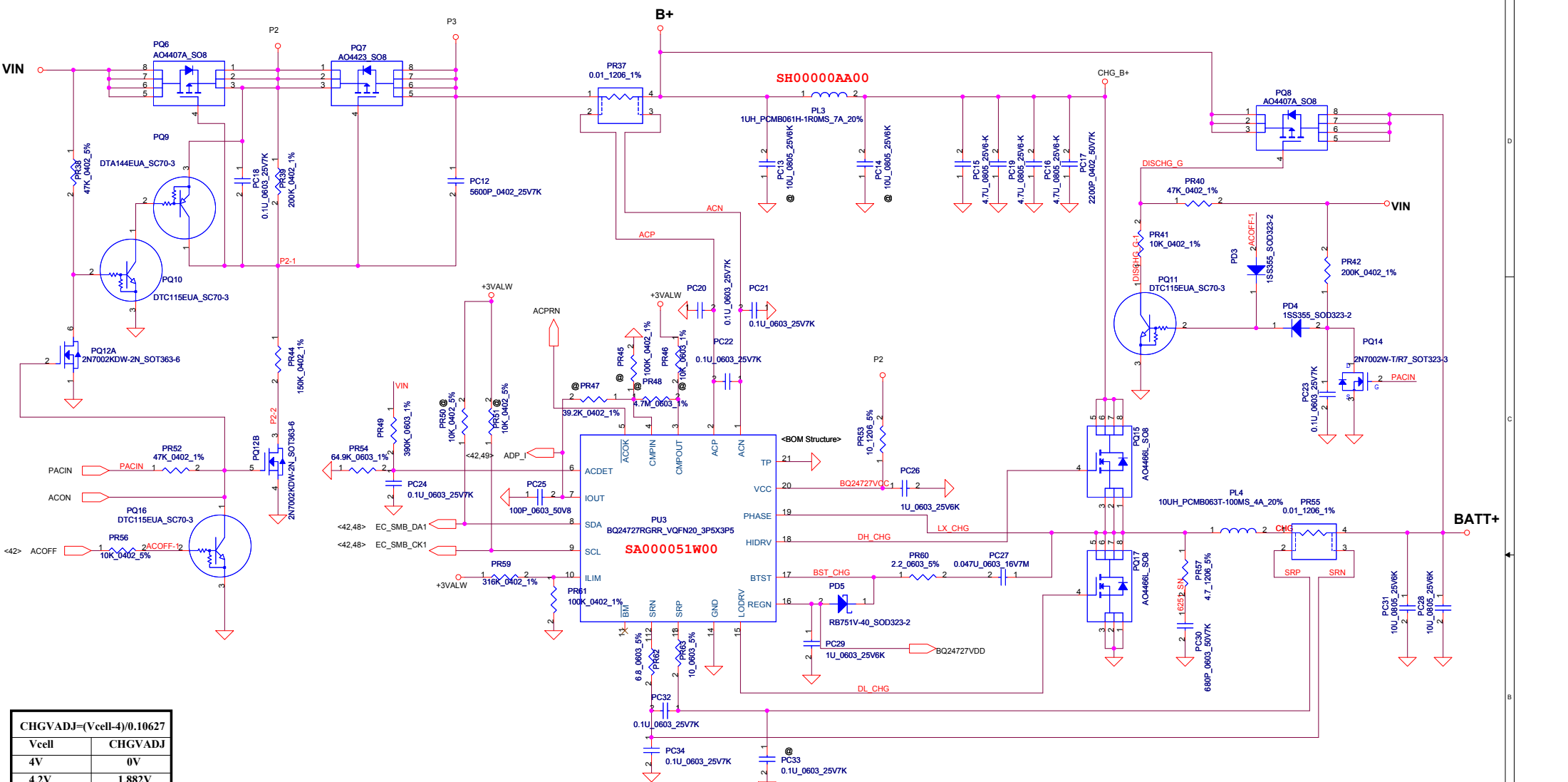
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR205  
PH201, PR205, PR211, PQ201, PR208, PR212



90W(DIS) : PR205=4.42K  
PR210=27.4K  
65W(UMA) : PR205=402(SD034020080)  
PR210=5.11K

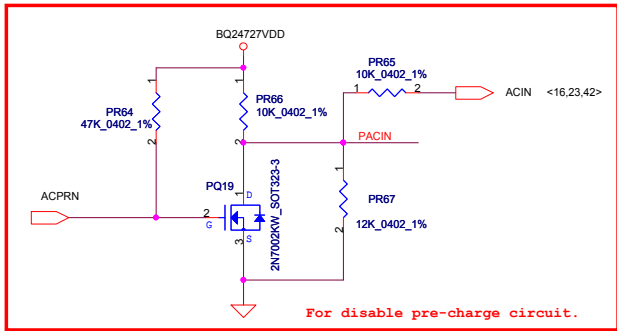


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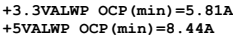
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A  
IREF=1.016\*Icharge  
IREF=0.254V~3.048V  
VCHLIM need over 95mV



For disable pre-charge circuit.

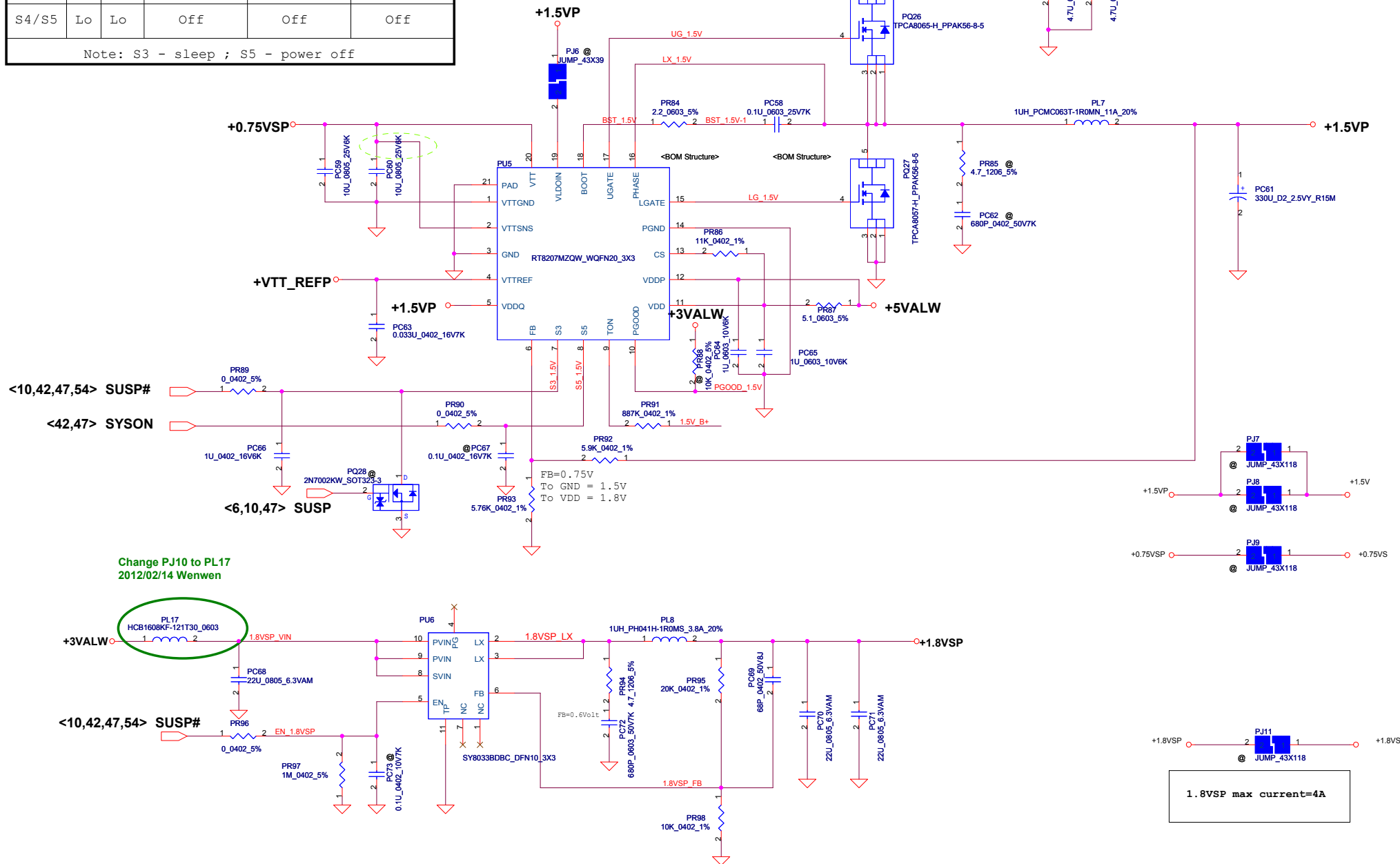
Change PJ2 to PL16  
2012/02/14 Wenwen



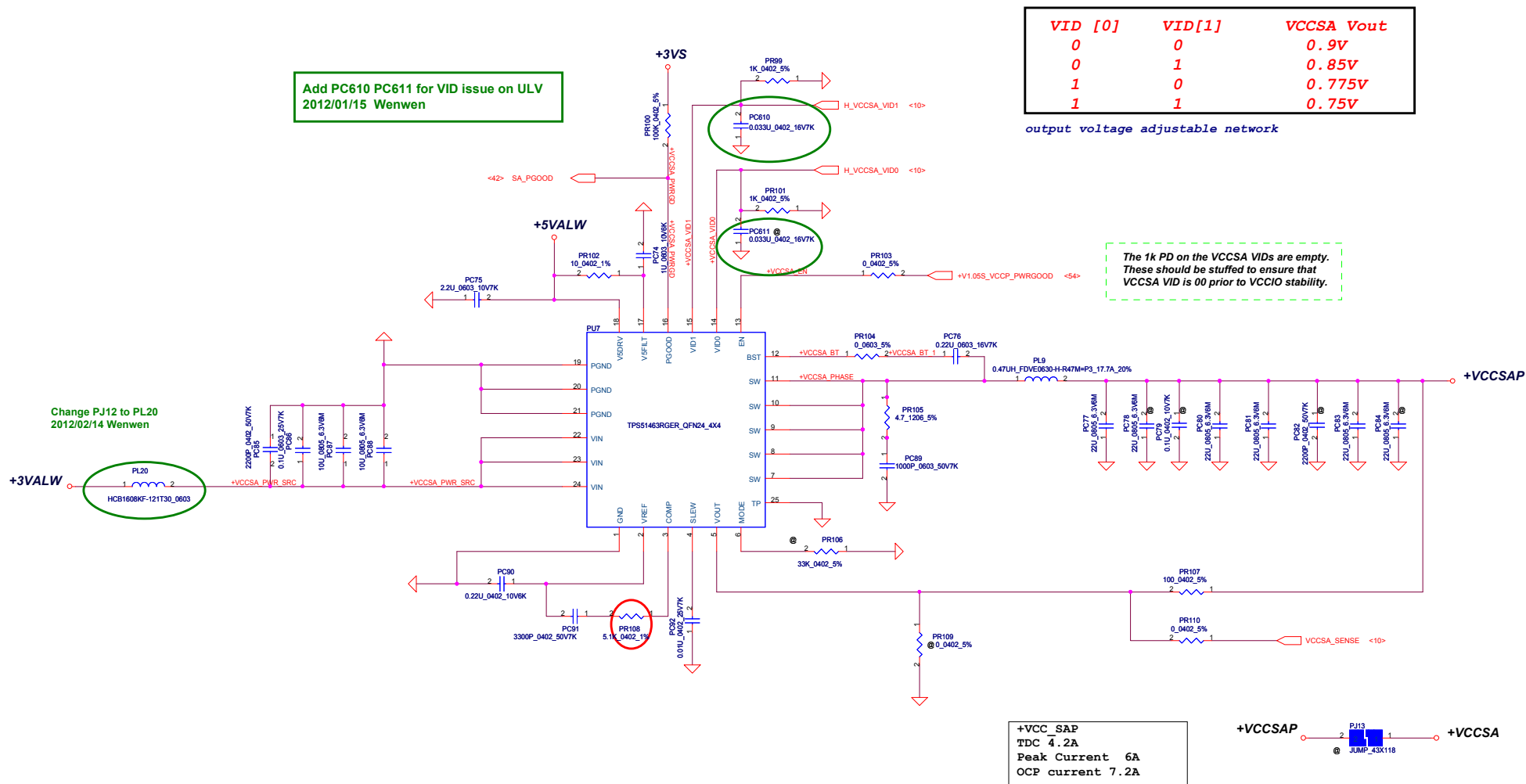
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> <b>PWR 3VALW/5VALW</b>	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



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Change PQ31 from TPCA8065 TO MDU1516  
Change PQ32 from TPCA8057-H to MDU1511  
2012/02/06 Wenwen

Add PQ41,PQ42 for heavy load (EDP Continuous current)  
2012/02/10 Wenwen

Change PL12 from SH000001K00 TO SH000001N00  
2012/02/07 Wenwen

Avoid high dV/dt

Connect to input caps

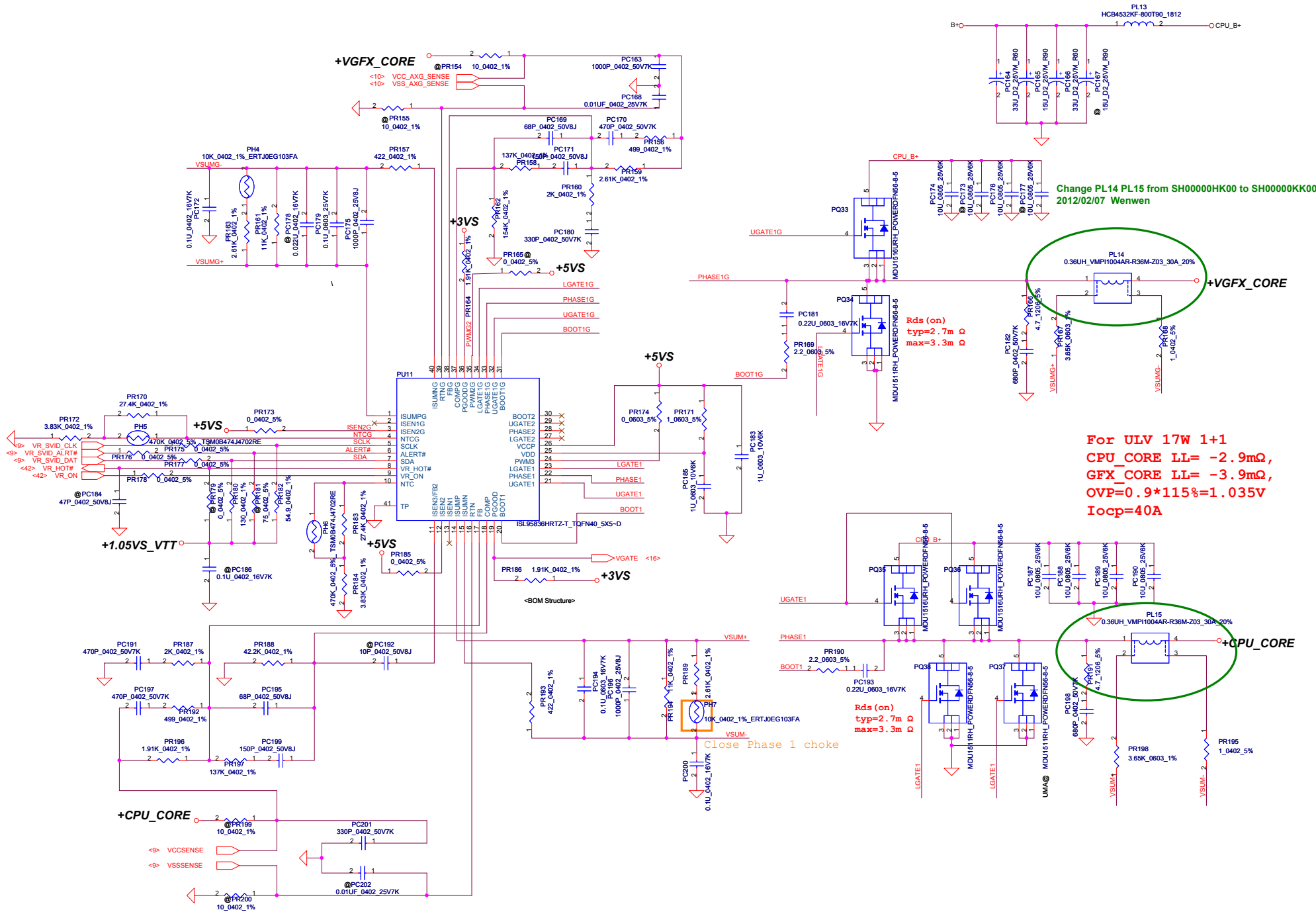
Shortest the net trace

+VGA\_CORE Near VGA Core

+VGA\_CORE Under VGA Chip

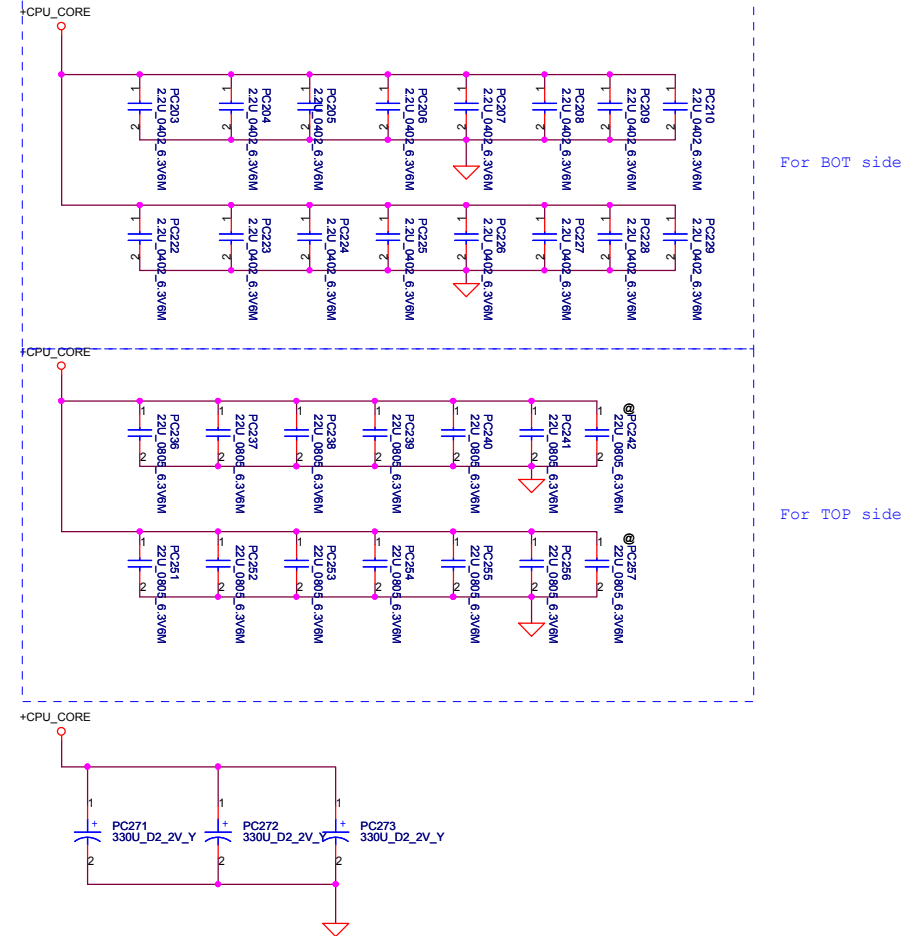
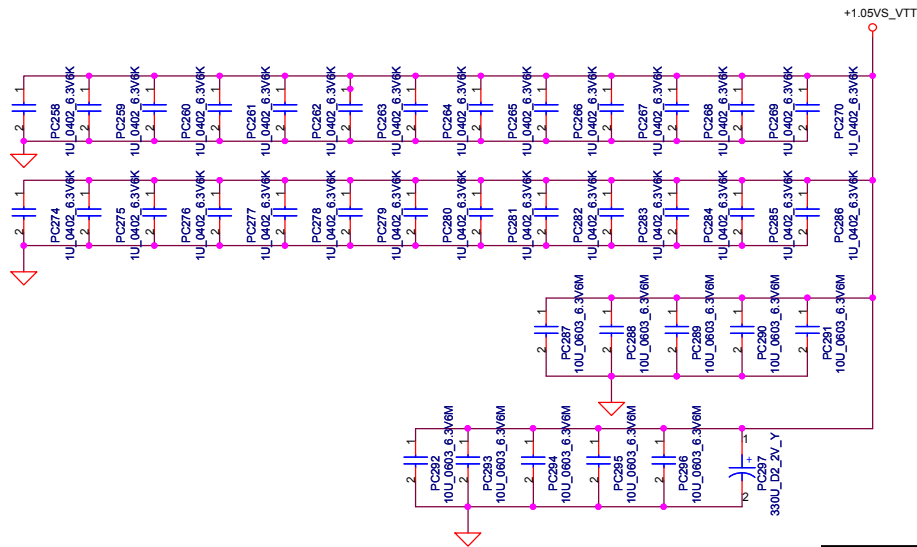
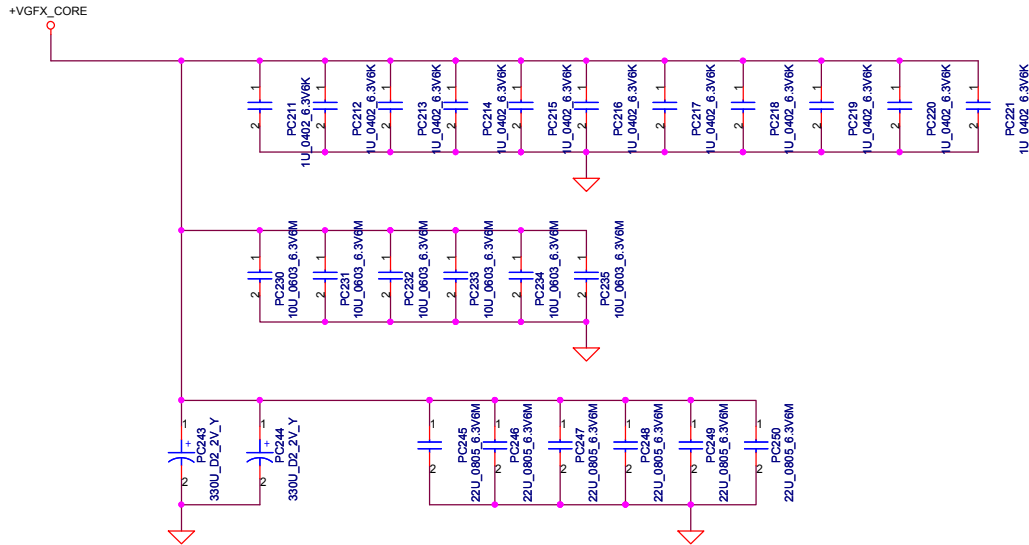
Add PC502 for NV GPU Spec request  
2012/02/03 Wenwen

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Title		Compal Electronics, Inc.	
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## Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add battery reset circuit	P47	add PJ401 PQ39 PR606 PC601 PC609 PR213 PR214 PQ40 PD303	2012/01/15	
2	For VCCSA VID issue on Intel ULV	P52	add PC601 PC611	2012/01/15	
3	Delete battery detector circuit	P48	delete PR24, PR28, PR26, PC8, PU2, PR31, PR33, PR25, PR22, PR32, PR23, PQ3, PQ4; delete PR43, PQ13; PR58, PQ18	2012/01/31	
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